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A universal fully reconfigurable 12-mode quantum photonic processor

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#### Abstract

PAPER

Photonic processors are pivotal for both quantum and classical information processing tasks using light. In particular, linear optical quantum information processing requires both large-scale and low-loss programmable photonic processors. In this paper, we report the demonstration of the largest universal quantum photonic processor to date: a low-loss 12-mode fully tunable linear interferometer with all-to-all mode coupling based on stoichiometric silicon nitride waveguides.

### 1. Introduction

Photonic processors, also called universal multiport interferometers (UMI) or photonic FPGAs, have attracted increasing attention in the past years for their many fields of applications such as quantum information processing based on linear optics [1-13], quantum repeater networks [14-17], (quantum) machine learning [18-22] and radio-frequency signal processing [23, 24]. A photonic processor is a tunable multimode interferometer which can achieve arbitrary linear optical transformations. Various realizations have been proposed in literature, where photonic processors have been arranged in many different topologies: triangular [1, 25], rhomboidal [4], fan-like [19], square [26], hexagonal [24] and quadratic [23].

Linear optics quantum information processing holds great promise for solving particular problems with exponentially greater computational power than classical computers. A large collection of proposed applications can be found in the literature [27–29]. The recent demonstration of a quantum advantage in a static optical system [30] shows the urgent need for programmable photonic processors.

The fundamental process of linear optics quantum information processing is quantum interference. To exploit it, a setup is needed consisting of photon sources, a photonic processor and single-photon detectors. The photons are used as information carriers and the photonic processor, formed by linear optical elements, will process quantum information by letting the photons interfere in a controlled manner. By looking at the configurations of the output samples of the detected photons, the result of the photonic computation can be read out.

For photonic quantum information processing, the requirements on a photonic processor are fourfold. First, it must be large-scale as this increases the complexity of the problems that can be solved. Second, it must be universal, since this enables the implementation of arbitrary transformations mapping the system onto various problems. For the universality, all-to-all connectivity (*n* inputs to *n* outputs) and full reconfigurability is necessary and sufficient to achieve *n*-dimensional universal transformations [1, 25, 26, 37]. Third, it must be low loss as otherwise the (quantum) information carried by single photons is lost. Finally, as stated above, a photonic processor needs to preserve quantum interference.

In this paper, we describe a 12-mode low-loss (end-to-end 5 dB) reconfigurable photonic processor based on stoichiometric silicon nitride waveguides, which is the largest universal photonic processor to date. We report the results of the classical and quantum characterization showing that full reconfigurability, low loss, and high-fidelity operations are achieved.



The paper is structured as follows: in section 2 the components of the 12-mode photonic processor are described; in section 3 we report the experimental results of the classical and quantum characterization of the processor; in section 4 prospects for the technology are discussed; in section 5 we derive the conclusions.

### 2. Photonic processor

In this section, we describe the main components of our 12-mode photonic processor (figure 1). It consists of three parts: an integrated silicon nitride photonic chip, peripheral equipment, and the software to control its functionality.

#### 2.1. Photonic chip

The heart of our photonic processor is a reconfigurable photonic integrated circuit based on stoichiometric silicon nitride  $(Si_3N_4)$  waveguides with the TripleX technology [31]. Thanks to the chosen material platform, we achieve propagation losses as low as 0.1 dB cm<sup>-1</sup> with a minimum bending radius of 100  $\mu$ m. The waveguide cross-section used in the photonic processor is an asymmetric double-stripe (ADS) [31] as shown in figure 1(a). The waveguides are designed for single-mode operation at a wavelength of 1550 nm. ADS waveguides enable low-loss coupling to standard telecom fibers using spot-size converters, where the upper silicon nitride stripe is removed by adiabatic tapering [31].

The reconfigurability of the photonic processor is achieved by exploiting the thermo-optic effect via resistive heating of 1 mm-long platinum phase shifters (PSs). Using these thermo-optic PSs, a  $\pi$  phase shift is achieved at  $V_{\pi} \cong 10$  V, corresponding to an electric power of ~385 mW per element.

The functional design of our processor is presented in figure 1(b). An optical unit cell, composed of a tunable beam splitter (TBS) (blue line) and a PS (red line) on the bottom output mode, is repeated 66 times over a square topology of 12 input/output modes<sup>3</sup> and circuit depth of 12. The circuit depth is defined as the

<sup>&</sup>lt;sup>3</sup> Throughout this paper, 'modes' refers to the zeroth order mode of each waveguide. We note that each waveguide supports multiple frequency modes.

maximum number of unit cells that an input mode encounters in the propagation direction of light. Twentyfour additional PSs are distributed across the inputs and outputs for sub-wavelength delay compensation and external phase tuning. In total, the processor contains 156 PSs. The TBSs are implemented by Mach–Zehnder interferometers (MZI) consisting of two 50:50 directional couplers (black lines in figure 1(b)) and an internal PS,  $\theta$ , followed by an external PS,  $\phi$ , at the bottom output mode. Each unit cell represents a node of the largescale interferometer where light can interfere [1, 25, 26, 37].

#### 2.2. Peripheral system

The photonic processor presented above is embedded in a control box that includes electronic and temperature control modules (figures 1(c) and (d)). The reconfigurable photonic integrated circuit is optically packaged with polarization-maintaining (PM) fiber arrays for the in- and out-coupling of light. For ease of access the input and output fibers are fixed to the front panel of the control box via PM mating sleeves. We measure an average loss for the 24 PM mating sleeves of about 0.18 dB/connector.

A printed circuit board (PCB) was fabricated and wire-bonded to the photonic processor. A total of 132 voltage drivers are connected to the PCB enabling the independent tuning of each thermo-optic PS, achieved via serial communication with a standard pc.

Temperature control and stability of the processor is achieved by active cooling. A thermo-electric Peltier element is placed beneath the sub-mount of the packaged processor, i.e., a metallic mount holding the processor, the fiber arrays and the PCB. The Peltier element favors the heat transfer in the vertical direction, from the on-chip PSs to the heat-sink. To further increase the cooling capacity of the system, water cooling can also be installed.

#### 2.3. Software—control system

The optical amplitude transmission through our photonic processor is given by  $E_{out} = \hat{S} E_{in}$ . The matrix  $\hat{S}$  is given by the product of two-mode matrices  $S_{m,n}$  of each unit cell between mode *m* and *n*. Considering a unit cell as in figure 1(b) with pairs of ideal and symmetric 50:50 directional couplers (k = 0.5), we find that

$$S_{\text{unit\_cell}}(\theta,\phi) = \frac{1}{2} \begin{pmatrix} 1 - e^{-i\theta} & -i(e^{-i\theta} + 1) \\ -i(e^{-i\theta} + 1)e^{-i\phi} & -(1 - e^{-i\theta})e^{-i\phi} \end{pmatrix}.$$

Rewriting the unit cell in terms of sine and cosine we find for the two-mode matrix of the full system

$$S_{m,n}(\theta,\phi) = \begin{pmatrix} 1 & 0 & \dots & \dots & \dots & 0 \\ 0 & \ddots & & & & \vdots \\ \vdots & e^{-i(\theta-\pi)/2} \sin \frac{\theta}{2} & -e^{-i(\theta-\pi)/2} \cos \frac{\theta}{2} & & \vdots \\ \vdots & -e^{-i(\theta-\pi)/2} e^{-i\phi} \cos \frac{\theta}{2} & -e^{-i(\theta-\pi)/2} e^{-i\phi} \sin \frac{\theta}{2} & & \vdots \\ \vdots & & & & \ddots & 0 \\ 0 & \dots & \dots & \dots & \dots & 0 & 1 \end{pmatrix},$$

where  $\theta$  is the internal phase of the MZI and  $\phi$  is the external phase. By varying  $\theta$  and  $\phi$  over  $2\pi$  it is possible to perform any transformation in the special unitary group, SU(2). It is important to note that the action of the processor is always described by the same classical transmission matrix *S* independently of the nature of the input state, i.e., either classical electric field amplitudes, photon-number states or other quantum states of light. Therefore, to know the transmission matrix, it is sufficient to characterize the processor classically. In the case of quantum input light, the formalism becomes  $\hat{a}_{out} = \tilde{S}\hat{a}_{in}$  where now the transmission matrix relates the ladder operators instead of classical electric field amplitudes [32].

The combination of quadratically many  $S_{m,n}$  allows the implementation of any complex-valued unitary transformation U. We can decompose any arbitrary unitary transformation U into sets of  $(\theta, \phi)_{m,n}$  belonging to specific unit cells between mode m and n of our processor [25, 26]. Assigning these  $(\theta, \phi)_{m,n}$  to the corresponding transmission matrix  $S_{m,n}$  and multiplying them in the order of light propagation through the processor, the exact optical response corresponding to U will be reproduced.

#### 2.4. Experimental setup

For classical characterization of the processor we use a CW diode laser at 1550 nm (2 mW output power—Thorlabs LP1550 PAD2). A PM fiber switch can be used to facilitate the procedure of characterization switching the input light across all the 12 inputs. For intensity measurements we use a set of InGaAs photodiodes each mounted on an FC/PC bulkhead (Thorlabs FGA01FC) (figure 2(a)). The output signal of



chip, light is detected by an array of 12 photodiodes, one per output channel. (b) A laser at 775 nm pumps a nonlinear PPKTP crystal, generating infrared collinear cross-polarized pair of photons. After polarization separation via a polarizing beam splitter, each single-photon impinges on a fiber-coupled collector (FC) and is injected into the chip. One of the collectors moves on a translational delay stage to temporally overlap the generated photons. The single photons at the output are detected with two SNSPD and coincidence measurements are performed.

the QuiX hardware, impinging on the PD array, is acquired and read out via an NI BNC-2090A and USB-6211 card.

For quantum characterization a 2 mm ppKTP crystal emitting collinear frequency-degenerate crosspolarized single-photon pairs is pumped with a Ti:sapphire (Tsunami, Spectra Physics) mode-locked laser with a center wavelength of 775 nm. Coupling between the light source and the QuiX hardware is done via polarization maintaining fibers. The photons at the output of the chip are detected with superconducting nanowire single-photon detectors (SNSPD).

## 3. Results

In this section, we report the classical and quantum characterization of the 12-mode photonic processor.

#### 3.1. Classical response

The classical characterization of the processor comprises the calibration of all the tunable elements and the total transmission of the processor, as shown in figures 3(a)-(c). Specific measurement protocols are used to characterize the TBS and PSs.

In figure 3(a) we show the calibration of one of the on-chip heaters as, for example, the one belonging to a TBS. Both outputs of the TBS are monitored while only the internal phase  $\theta$  is varied (inset figure 1(b)). This is done by applying a varying voltage, V, to the thermo-optic PS. The same procedure is adopted for characterizing the PSs. By following a specific order, we characterize the entire processor and find that all the 132 thermo-optic PSs are tunable over more than  $2\pi$  phase range with high extinction ratio. In this way, we achieve full control over the processor.

In figure 3(b), we report the insertion loss matrix of the processor. The insertion loss matrix includes both the fiber-to-chip-to-fiber coupling losses and the on-chip propagation loss. It excludes thus the aforementioned connector loss of 0.18 dB/connector. The reader can clearly see that there is one input channel that shows higher losses than the others. This is confirmed by inspection of one of the fibers, which turned out to be damaged. The optimal transmission for this input channel can be easily retrieved by exchanging the damaged fiber. On average, excluding the damaged channel, the processor shows an insertion loss of  $\sim$ 5 dB where  $\sim$ 0.8 dB comes from propagation loss and the remaining  $\sim$ 4.2 dB are coupling losses.



The two outputs is plotted and fitted versus the internal phase  $\theta$  and the applied voltage. A  $V_{\pi} \cong 10.4$  V is measured. (b) Setup transmission for each input–output combination. (c) Theory vs experimental realization of one random permutation matrix P, X6 and one switching matrix S (between mode 1 and 7) with fidelities of respectively 0.955, 0.940 and 0.984. (d) Fidelity distribution of 1000 Haar random matrices. (e) Measured Q and X unitary transformation with fidelities 0.922 and 0.930, respectively. Intensity is normalized to its maximum for this measurement.

Finally, to confirm the universality and control of the processor, we perform a large variety of  $12 \times 12$  unitary transformations as summarized in figures 3(c)-(e). For each target transformation  $U_i$ , we measure the corresponding experimental output intensity distribution  $|U_{exp}|^2$ . We compare the experimental results, normalized to the input/output coupling efficiency, with the target intensity output distribution  $|U_i|^2$  via the fidelity  $\mathcal{F}_i = \frac{1}{D} \operatorname{Tr}(|U_i^{\dagger}| \cdot |U_{exp}^{\text{norm}}|)$ , where D is the dimension of the unitary transformation and of our processor, i.e., D = 12. Note that the calculated fidelity is an amplitude fidelity therefore not taking into account the phases of the unitary transformation elements.

We perform unitary transformations spanning various applications such as permutation (P), Haar-random matrices, high-dimensional Pauli-X gates (X) and optical switching matrices (S). Furthermore, to ultimately illustrate our full control over our processor we implement the letters Q and X of our company name QuiX.

In figure 3(c), we report, as an example, the target (theory)  $P_{\text{th}}$ ,  $X_{\text{th}}$  and  $S_{\text{th}}$  matrix (top row from left to right) and their corresponding experimental implementations (bottom row). Figure 3(d) shows the fidelity

Table 1. Summary of measured fidelities.

	#	$\mathcal{F}_{ m ave} \pm \sigma$
Random perm	12	$0.930\pm0.013$
Pauli- $X^{n=0,\dots,12}$	12	$0.945\pm0.007$
Switching	12	$0.985\pm0.006$
Haar random	1000	$0.904\pm0.024$
Logo	2	$0.926\pm0.004$



distribution of 1000 Haar random unitaries. We note that an increase in the complexity of the optical transformation is associated with a decrease in fidelity, as is natural to expect. Since, by definition, Haar matrices cover the space of unitary transformations in a uniform way, we expect the fidelity for this set to be representative for an arbitrary transformation. Finally, figure 3(e) reports the measurements of the first and last letter of the company name QuiX. The results are summarized in table 1.

## 3.2. Quantum response

After having demonstrated full control of the processor via the classical response characterization, we attach the QuiX hardware to the quantum light source as shown in figure 2(b). Quantum interference experiments were performed across the whole photonic processor evaluating to what extent the processor preserves the indistinguishability of the input single photons. This measurement tests all sources of induced distinguishability on the single photons, such as path-dependent dispersion.

The single-photon source is characterized separately by running a Hong–Ou–Mandel (HOM) [33] interference experiment over a tunable fiber splitter that gives a visibility of 0.93. By choosing inputs pairwise, we run HOM interference experiments on every single TBS on the processor (figure 4). The average visibility of the

on-chip HOM interference dips is calculate as  $vis_{ave} = \sum_{n} \frac{\left(1 - \frac{cc_{ind}}{cc_{dist}}\right)_{n}}{n_{tot}}$  where  $n_{tot} = 66$ , where  $cc_{ind/dist}$  is the coincidence count rate for indistinguishable or distinguishable photons (as indicated in figure 4). We obtain an average visibility of  $vis_{ave} = 0.923$ . We observe from figure 4(c) that the distribution of the HOM visibility

is rather random across the UMI confirming the absence of any systematic error in the processor. Some TBSs, e.g., #136, 140 and 145, present a low visibility of the quantum interfere: this is due to an imperfectly optimized 50:50 splitting ratio setting of these TBSs, which reduces the HOM visibility.

Comparing the reference HOM dip visibility measured outside the chip of  $\sim$ 93% and the measured average on-chip visibility we can conclude that the processor does not affect the spectral-temporal indistinguishability of the signal and idler photons coming from the single-photon source. The on-chip visibility is ultimately limited by the source itself.

## 4. Discussion

Finally, we discuss the prospects of our technology. With this  $12 \times 12$  processor, we have not exhausted the capabilities of the Si<sub>3</sub>N<sub>4</sub> platform; we anticipate producing larger processors with higher fidelity and lower optical loss in the future. We discuss these issues in turn.

The fidelity of the unitary transformations can be improved by correcting and compensating for crosstalk. To tackle the crosstalk there are both hardware and the software solutions. Examples can be found in the literature [34–36]. Furthermore, the compensation of non-ideal extinction ratio of the TBS will also improve the fidelity. This can be done by adding redundancy to the waveguide mesh [37, 38].

The insertion loss of the system can be further reduced by optimal waveguide engineering, to enable an even greater scalability of our technology. By optimal waveguide tapering the coupling losses can be reduced down to  $\sim 1$  dB [31]. With these modifications, the system will become practical as a photonic processor for quantum interference experiments in the regime where a quantum advantage exists [30]. The integration of single-photon sources, by exploiting the third-order nonlinearity of silicon nitride, and detectors will help further in reducing the coupling losses [39–41].

Valid alternatives to thermo-optic tuning are available such as the implementation of liquid crystals [42, 43], phase-changing materials [44] and stress-optic tuning [45, 46] to reduce the power consumption. The latter additionally has the advantage to operate at cryogenic temperatures [47]. Operating the chip at cryogenic temperatures would permit direct integration with both solid-state single-photon sources [48] and superconducting single-photon detectors [40, 41].

To reduce the footprint of the unit cell, alternative approaches can be undertaken, e.g., by dual-drive directional couplers [49], dual-drive MZI [5] and MEMS [50].

Finally, we would like to comment on two aspects of the time-budget of our current system: the speed of reconfigurability and the runtime of simple quantum computations.

The speed of reconfigurability of our processor is determined by both the thermo-optic tuning mechanism, that works on the millisecond time scale, and the control peripheral electronics that reconfigure the whole processor in about 1 s via serial communication. The reconfigurability speed could be optimized to the thermal limit of milliseconds by a redesign of the peripheral electronic system implementing, e.g., parallel communication.

The runtime of simple quantum computations strongly depends on the type of computation and the photons collecting statistics. In the case of a Boson sampling experiment, obtaining samples of the output distribution takes only few nanoseconds, i.e., the travel time of the photons through the processor. The production of such samples, however, is limited by the coincidence rate one can measure, currently 100 Hz for heralded three-photons coincidences, which is ultimately limited by the probability of synchronous generation of photon pairs from two independent SPDC sources ( $\sim 2\%$ ) and not by the transmission of the processor. For this reason, scaling up the system to higher number of photons requires more efficient single photon sources, such as quantum dots.

## 5. Conclusion

In this paper we have reported a 12-mode fully reconfigurable universal photonic processor based on silicon nitride waveguides. The processor is embedded into a control system that enables remote access to its optical functionality and reconfigurability. The system operates at 1550 nm with insertion loss of ~5 dB (averaged over all the optical paths). All the 132 tunable elements of the processor provide more than  $2\pi$  phase shift with high extinction ratio. High fidelities are measured over a set of 1036 unitary transformations. Quantum interference of high visibility is replicable across the entire processor, i.e., the indistinguishability of photons is preserved.

The photonic processor presented here is the largest low-loss plug-and-play universal square photonic processor to date, enabling fully reconfigurable unitary transformations across 12 inputs and through 12 layers of depth.

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## Data availability statement

The data generated and/or analysed during the current study are not publicly available for legal/ethical reasons but are available from the corresponding author on reasonable request.

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