LS2085A RDB Reference Manual

LS2085ARDBRM
Rev. X3, 02/2015

freescale™

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: LS2085ARDBRM
Rev. X3, 02/2015

Contents

List of Figures

List of Tables

Chapter 1
Introduction

The LS2085A Reference Design Board (RDB) is a high-performance computing, evaluation, and development platform that supports the QorIQ™ LS2085A LayerScape Architecture processor. The LS2085A provides SW development platform for the Freescale LS2085A processor series, with a complete debugging environment. The LS2085A RDB is lead-free and RoHS-compliant.

NOTE

The LS2085A RDB is ordered using the part number LS2085A RDB.

Developers using LS2085A RDB onboard resources and debugging devices can perform the following:

- Upload and run code
- Set breakpoints
- Display memory and registers
- Connect and incorporate proprietary hardware into target systems using the LS2085A as a host processor
- Use the LS2085A RDB as a demonstration tool

A software application developed for the LS2085A RDB can run with various input/output data streams, for example PCIe, XFI or SATA connections.

The board support package (BSP) is developed using the Linux operating system.

Figure 1-1 shows the LS2085A processor block diagram.

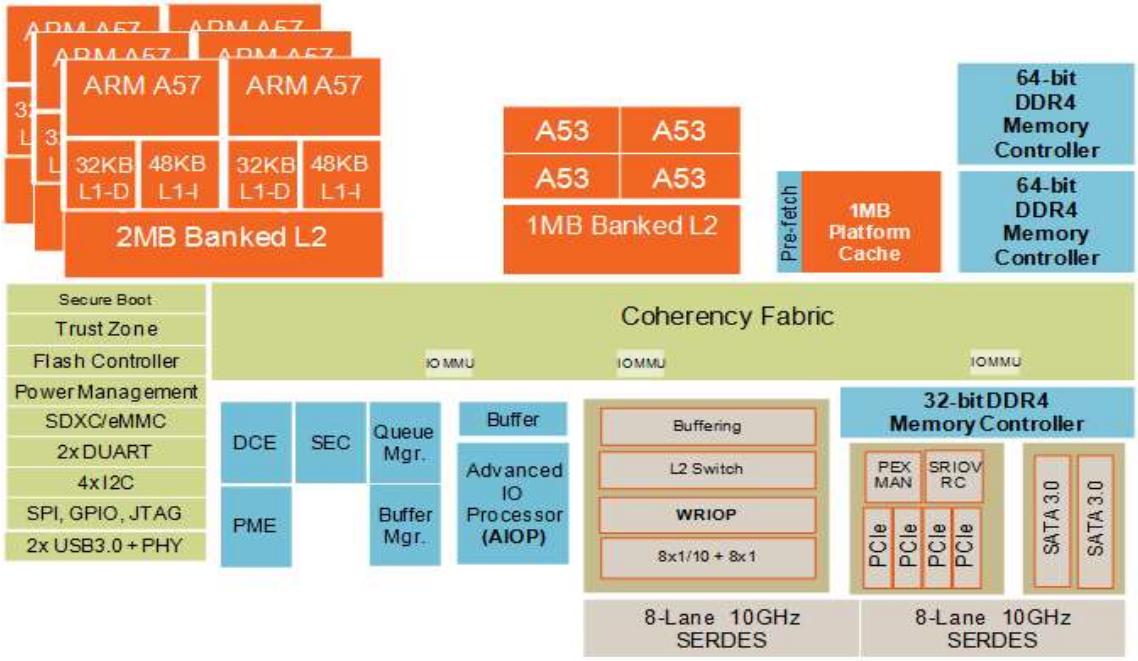


Figure 1-1. LS2085A Processor block diagram

1.1 Related documents

Table 1-1 lists the additional documents that you can refer to, for more information on LS2085A RDB.

Some of these documents may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1-1. Related documents

Document	Description
LS2085A RDB Quick Start Guide	Describes the LS2085A RDB hardware kit, and lists the settings required to connect switches, connectors, jumpers, push buttons, and LEDs to the peripheral devices.
LS2085A Integrated Multicore Communication Processor Family Reference Manual	Provides a detailed description of the LS2085A multicore processor and of some of its features like memory mapping, serial interfaces, power supply, chip features, and clock information.
LS2085A LayerScape Advanced Multicore Processor Data Sheet	Contains LS2085A information on Pin assignments, Electrical characteristics, Hardware design, considerations, Package information, and Ordering information.
LS2085A Chip Errata	Lists the details of all known silicon errata for LS2085A.
International Rectifier IR3565B Datasheet	Describes the digital POL buck controller with I2C and PMBus interface. IR3565B is a dual power supply regulator generating VDD & GVDD for the LS2085A device.

NOTE

Freescale Semiconductor, Inc. does not own *International Rectifier IR3565B Datasheet* and it is mentioned solely for the reference purpose.

1.2 Acronyms

The following table lists the acronyms used in the document.

Table 1-2. Acronyms

Term	Meaning
ATX	Advanced Technology Extended (power supply)
AVDD	Core, Platform, DDR and SerDes PLL's supply voltages
BRDCFG	Board Configuration
CLKIN	Clock Input (interchangeable with SYSCLK)
COP	Common On-Chip Processor
CSR	Control Status Register
CVDD	eSPI block supply voltage
DDR	Double Data Rate
DRAM	Dynamic Random Access Memory
DVDD	UART/I2C/DMA supply voltage
ECC	Error Detection and Correction
EEPROM	Electrically Erasable Programmable ROM
EMI	ElectroMagnetic Interference
eMMC	Embedded Multi Media Card
eSDHC	Enhanced Secure Digital High Capacity Card
FCM	NAND Flash Control Machine
Fman	Frame Manager
FPGA	Field Programmable Gate Array
GETH	Giga Ethernet (GbE)
GPINPUT	General Purpose Input
GPIO	General Purpose In/Out
G1VDD	DDR module supply Voltage
HRESET	Hard Reset
I^2C	Inter-Integrated Circuit Multi-Master Serial Computer Bus
IPL	Initial Program Load
JTAG	Joint Test Access Group (IEEE® Std. 1149.1™)
LBMAP	Local Bus Map
LED	Light-emitting Diode

Table 1-2. Acronyms

Term	Meaning
LSB	Least Significant Bit
LVDD	GETH block supply voltage
MMC	Multi-media Card
MSB	Most Significant Bit
OCM	Off-line Configuration Manager (FPGA-embedded)
OVDD	General I/O supply voltage
PLL	Phased Lock Loop
POVDD	PROG_SFP (Security Fuse Programming Override supply Voltage)
ppm	Parts per Million
PROMJet	Memory Emulator by EmuTec Inc.
RCW	Reset Configuration Word
REF CLK	Reference Clock (Clock Synthesizer Input Value)
RGMII	Reduced General Media Independent Interface
ROM	Read Only Memory
RTC	Real-time Clock
SATA	Serial Advanced Technology Attachment
SCL/SCLK	Serial Clock
SD	Secure Digital Card
SDHC	Secure Digital High Capacity
SDREFCLK	SerDes Reference Clock
SERCLK	SerDes Clock
SerDes (SRDS)	Serializer/Deserializer; for example PEX, XAUI, SGMII, SATA, sRIO, AURORA, and XFI
SGMII	Serial Gigabit Media Independent Interface
SMB	Subminiature Version B Connector
SPI	Serial Peripheral Interface Flash
SRAM	Static Random Access Memory
SVDD	SerDes1 and SerDes2 core logic supply voltage
SYSCLK	System Clock
TAP	Test Access Port; for example, USB TAP or ETH TAP
TESTSEL	Test Select

Table 1-2. Acronyms

Term	Meaning
TH_VDD	Thermal Monitor unit supply voltage
TRIG_IN/OUT	Trigger In/Out
UART	Universal Asynchronous Receiver/Transmitter
uDIMM	Unbuffered Dual In-Line Memory Module Form Factor
USB	Universal Serial Bus
USBCLK	USB Clock
VDD	Core and Platform supply voltage
VDD_LP	Low Power Security Monitor supply voltage
XAUI	Ten Attachment Unit Interface
XVDD	SerDes1 and SerDes2 transceiver supply voltage

1.3 Features

Table 1-3 lists the features of LS2085A RDB.

Table 1-3. LS2085A RDB features

LS2085A RDB Feature	Specification	Description
Processor Support	Core Processors	8x64-bit up to 1.8 GHz ARM A57 cores
	HighSpeed Serial Ports (SerDes)[1]	• 8 lanes, up to 10.3125 GHz SerDes • Supports PCIe 3.0, SATA 3.0,and XFI. • Two PCIe connectors supporting: 1. PCIe card (x4/x8) 2. PCIe card (x4) • Two SATA connectors • Four RJ45 connectors for Ethernet 10G support • Four SFP+ cages for XFI support

Table 1-3. LS2085A RDB features

LS2085A RDB Feature	Specification	Description
	DDR	• Two ports of 72-bits (8-bits ECC) DDR4. Each port supports two DIMM connectors. One port has four chip-selects while the second port has two chip-selects. Support is up to 2133MT/s. • One port of 40-bits (8-bits ECC) DDR4 which supports four chip-selects and one DIMM connectors. The DIMM has two chip selects that are selectable from the four LS2085 chip select. Support is up to 1600MT/s. • Each DIMM connector supports DDR4 uDIMM or RDIMM memory modules. • Each DIMM connector supports single/dual rank DDR4 memory modules. • First DIMM connector in each port can support Quad rank DDR4 memory modules. • Default memory module is 8GB, 72-bit, dual rank DDR4 uDIMM running up to 2133MT/s
	1588	• Support through on-board header (JP4)
	USB 3.0	• Two high speed USB 3.0 ports • First USB 3.0 port configured as Host with Type-A connector (CN1). • Second USB 3.0 port configured as OTG with micro-AB connector (CN2).
	IFC	• IFC rev. 2.0 implementation supporting ***Little Endian*** connection scheme. • CPLD connection • One 128 MB NOR flash 16-bit data bus (1.8V) • One 2 GB NAND flash with ECC support (3.3V) connected behind the CPLD to do IFC bus voltage translation
	eSDHC	SD connector (CN3) is used for the following add-in card types: • SD Card Rev 2.0 and Rev 3.0
	SPI	• 64 MB high-speed flash memory for boot code and storage (up to 108MHz in single transfer rate mode) • 512 KB high-speed flash memory (up to 85 MHz) for storing image to be used by the Aquantia PHY AQR405 internal microcontroller.
	Multimaster Serial Bus, I^2C,	Use two controllers
	DUART (2/channel)	• One DB9 D-Type connector (P1) with dual UART port connection
	SATA (2 channels)	Two SATA onboard connectors (CON2 and CON3)
	Package	• 1396-pin, Flip-Chip PBGA of 37x37mm 1.0mm pitch • Socket and heatsink included

Table 1-3. LS2085A RDB features

LS2085A RDB Feature	Specification	Description
System Logic	CPLD	• Manages the following: – system reset sequencing – system and SerDes clock speed selections – boot and RCW source selection • Implements registers for system control and monitoring • General fault monitoring and logging • Runs from ATX-PS hot power rails, allowing operation while system is off.
Clocks	SYSCLK	• Software programmable in 333.333 kHz increments from (83.3-133.33) MHz
	SerDes	• Supports four domains • 100 (Spread Spectrum optionally), 125 and 156.25 MHz configurations support PCIe, SATA, SGMII, XFI and XAUI
	Ethernet	• Supports 125 MHz ethernet clock for1588
	RTC	• Supports 32KHz LS2085A Real Time Clock input
Power Supplies	One dedicated programmable regulator supplying LS2085A core and DDR power domains. Set of independent DC/DC and LDO power supplies	• PMBus control • Power: – 1.0V for USB Core – 1.8V for LS2085A PROG_SFP and PROG_MTR (POVDD) – 1.8V AND 3.3V for CPLD – 1.35 XVDD – 1.0V SVDD – 1.8V for LS2085A General I/O – 1.8V UART/I2C – 1.8V for USB HVDD – VTT/VREF for DDR4 – 1.8 for eSPI – 3.3V eSDHC – 1.0V for Secure monitor (VDD_LP)

[1] SerDes is an integrated circuit transceiver that converts parallel to serial data, and vice versa.

1.4 LS2085A block diagram

Figure 1-2 shows LS2085A RDB block diagram.

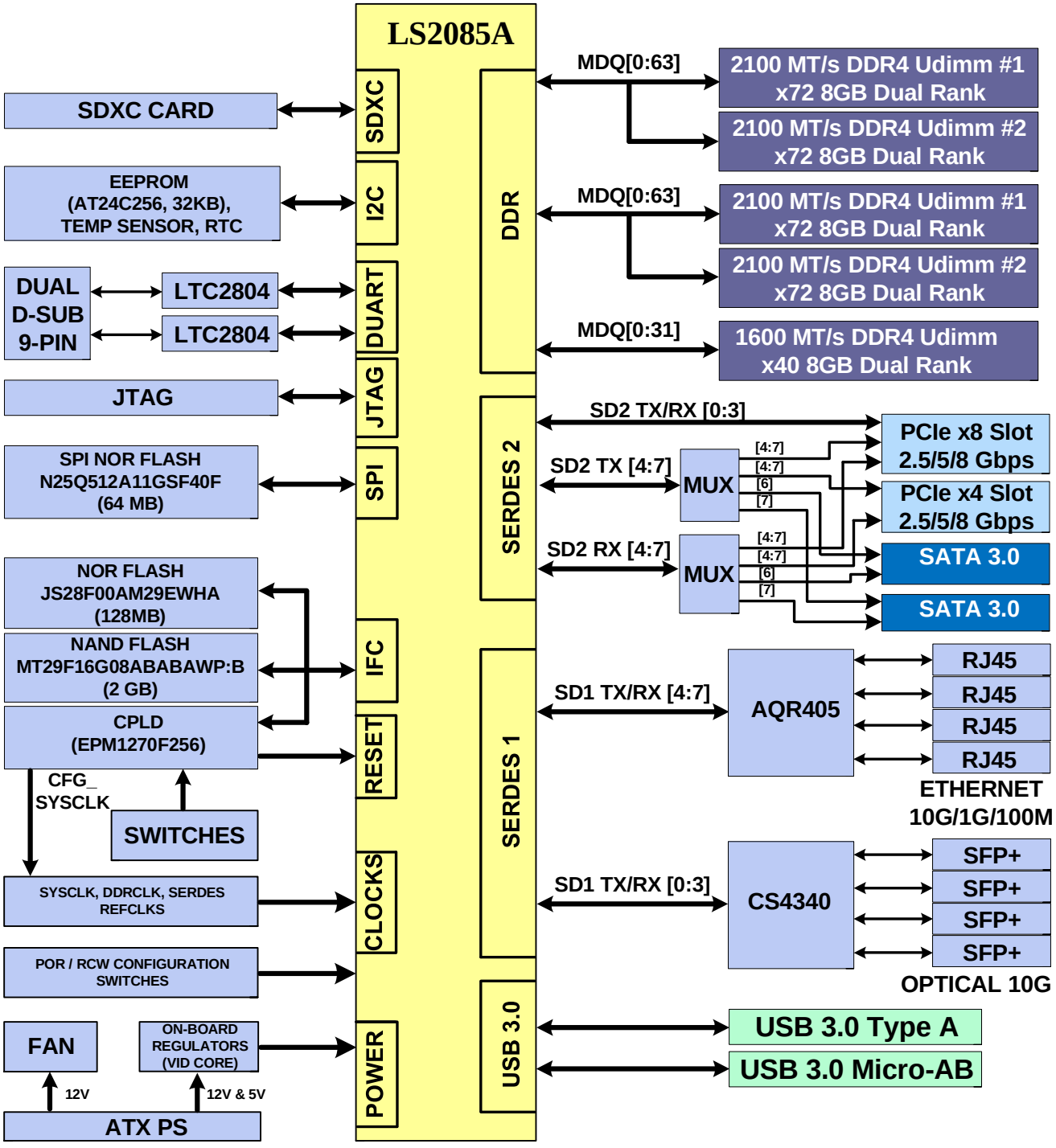
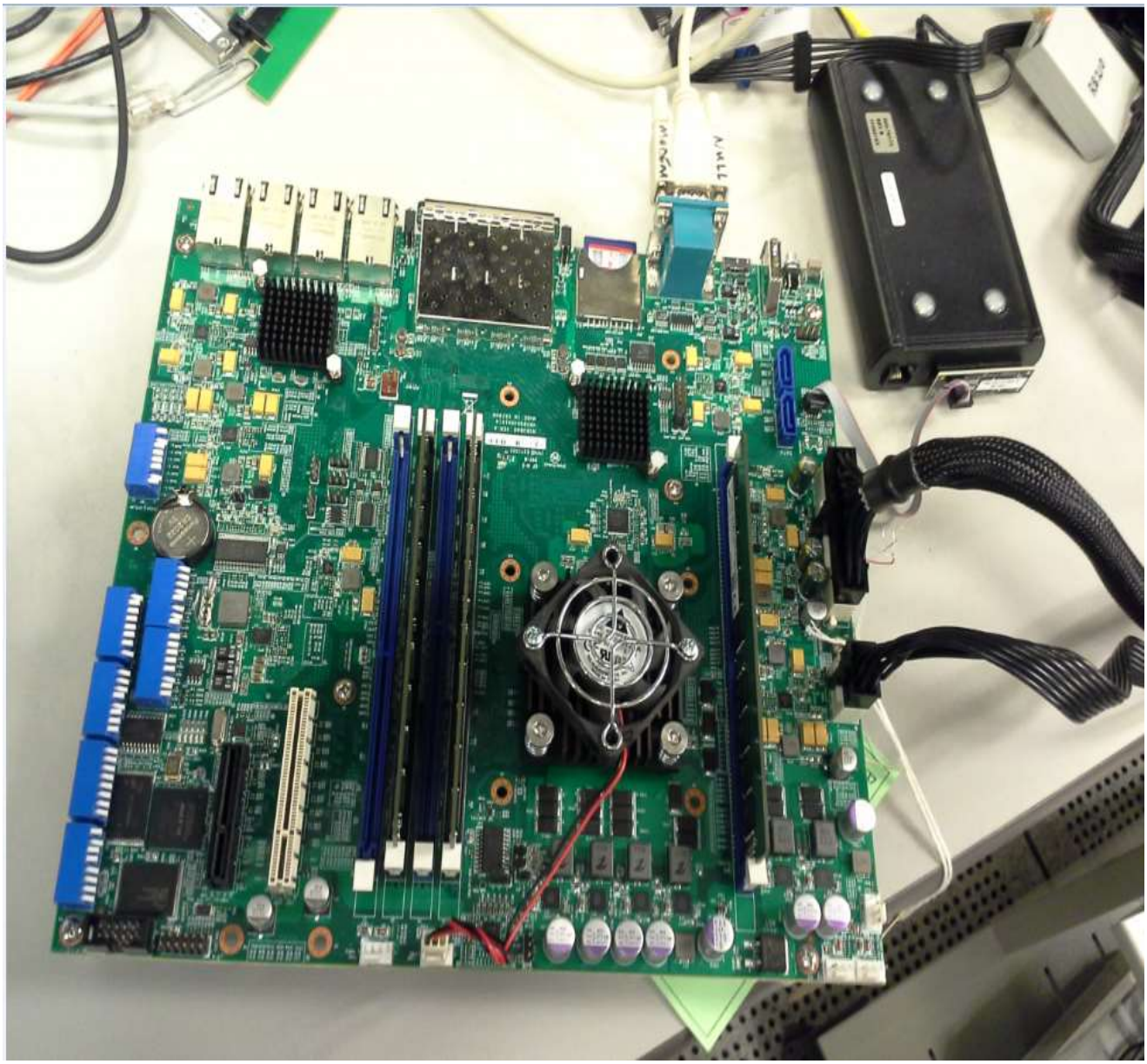


Figure 1-2. LS2085A RDB block diagram

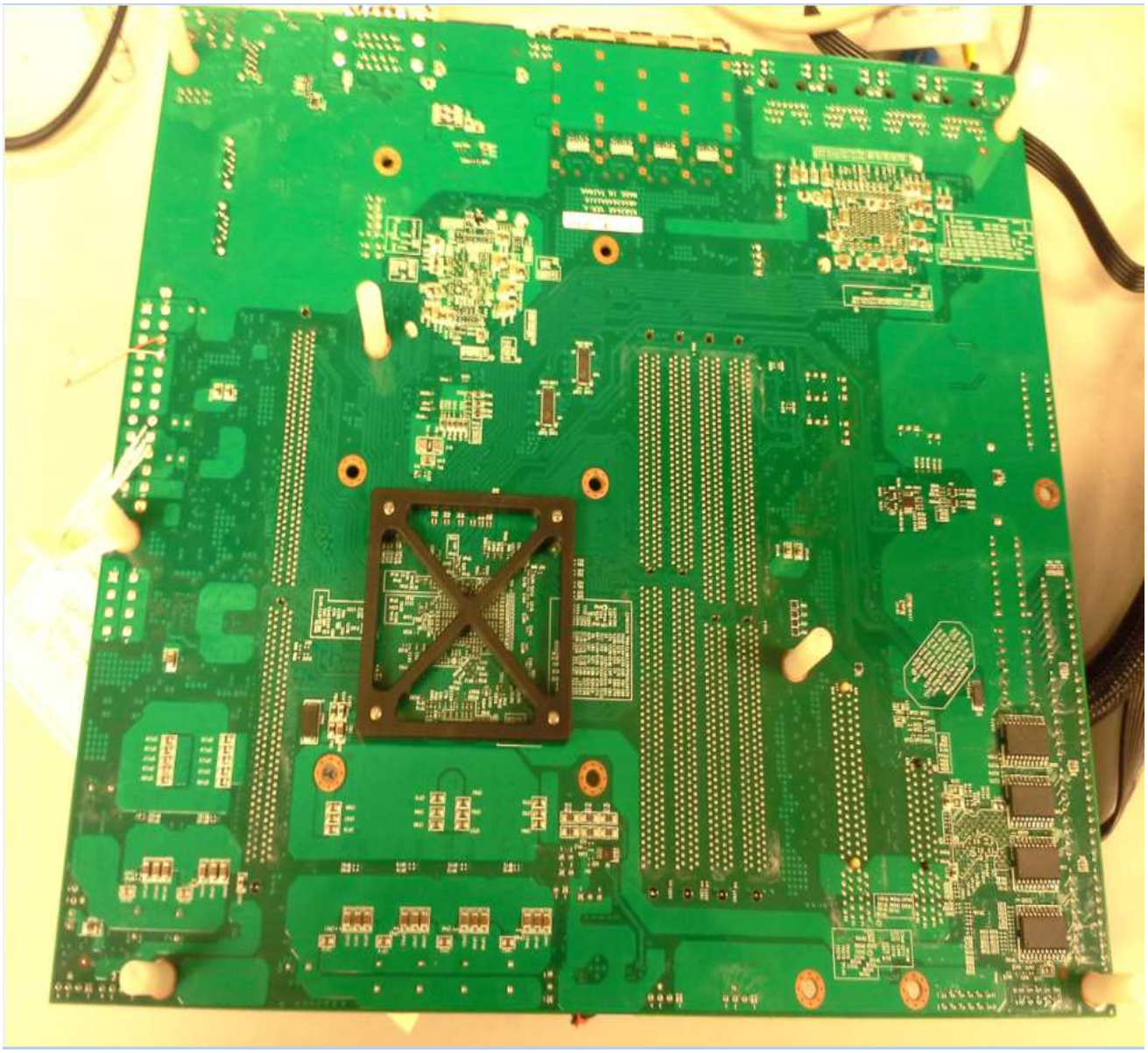
1.5 LS2085A RDB board drawings

In this section:

1.5.1 LS2085A RDB Top Side View



1.5.2 LS2085 RDB Bottom Side View



1.6 Development system usage

The LS2085A RDB functions as a desktop computer and operates as a development and evaluation system.

Chapter 2 Rev. X3 Functional Description

The LS2085A RDB architecture is primarily determined by the LS2085A LayerScape Architecture processor with the need to evaluate LS2085A processor features and to test its ability to deliver an easily usable off-the-shelf software development platform.

2.1 Double Data Rate (DDR)

The LS2085A contains a number of DDR-related features:

- Two ports (D1, D2) of DDR4, each supporting the following:
  - 64-bit data, 8-bit ECC
  - Operating at up to 2133 MT/s
  - Four chip-selects
  - Two DIMM connectors each supporting single and dual rank industry-standard, 288-pin JEDEC DDR4 uDIMM modules
  - Support for x4, x8 and x16 DDR4 memory devices
- One port (D3) of DDR4 supporting the following:
  - 32-bit data, 8-bit ECC
  - Operating at up to 1600 MT/s
  - Four chip-selects
  - Two DIMM connectors each supporting single and dual rank industry-standard, 288-pin JEDEC DDR4 uDIMM modules
  - Support for x8 and x16 DDR4 memory devices
- Default uDIMM used on the first two ports (D1, D2) is dual rank, 8GByte, 64-bit with ECC operating @ 2133MT/s data rate.
- Default uDIMM used on the third port (D3) is dual rank, 8GByte, 64-bit with ECC, 2133MT/s module operating @ 1600 MT/s data rate.
- On port D3, only 32-bits are connected with 8-bit ECC (for a total of 2GByte)
- Memory interface includes all necessary termination and IO power and is routed in order to achieve maximum performance on the memory bus.

NOTE

The LS2085A RDB board supports all types, ranks, and speeds of uDIMM's. However, all the combinations do not exist in the uDIMM market, so the system is shipped with a *representative* uDIMM.

Figure 2-1 shows DDR port D1 memory architecture.

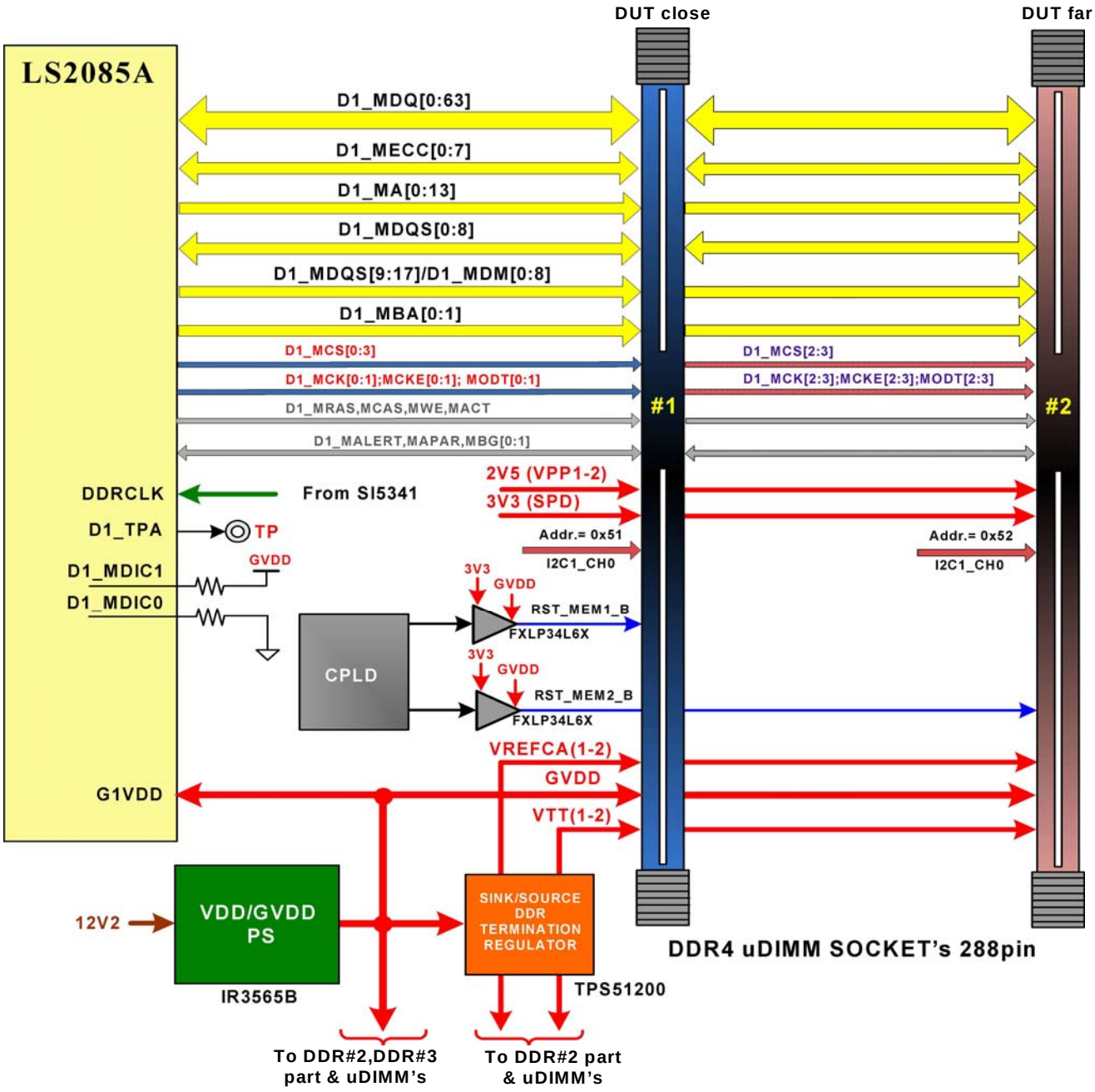


Figure 2-1. LS2085A RDB DDR Port D1 interface

Figure 2-2 shows DDR port D2 memory architecture.

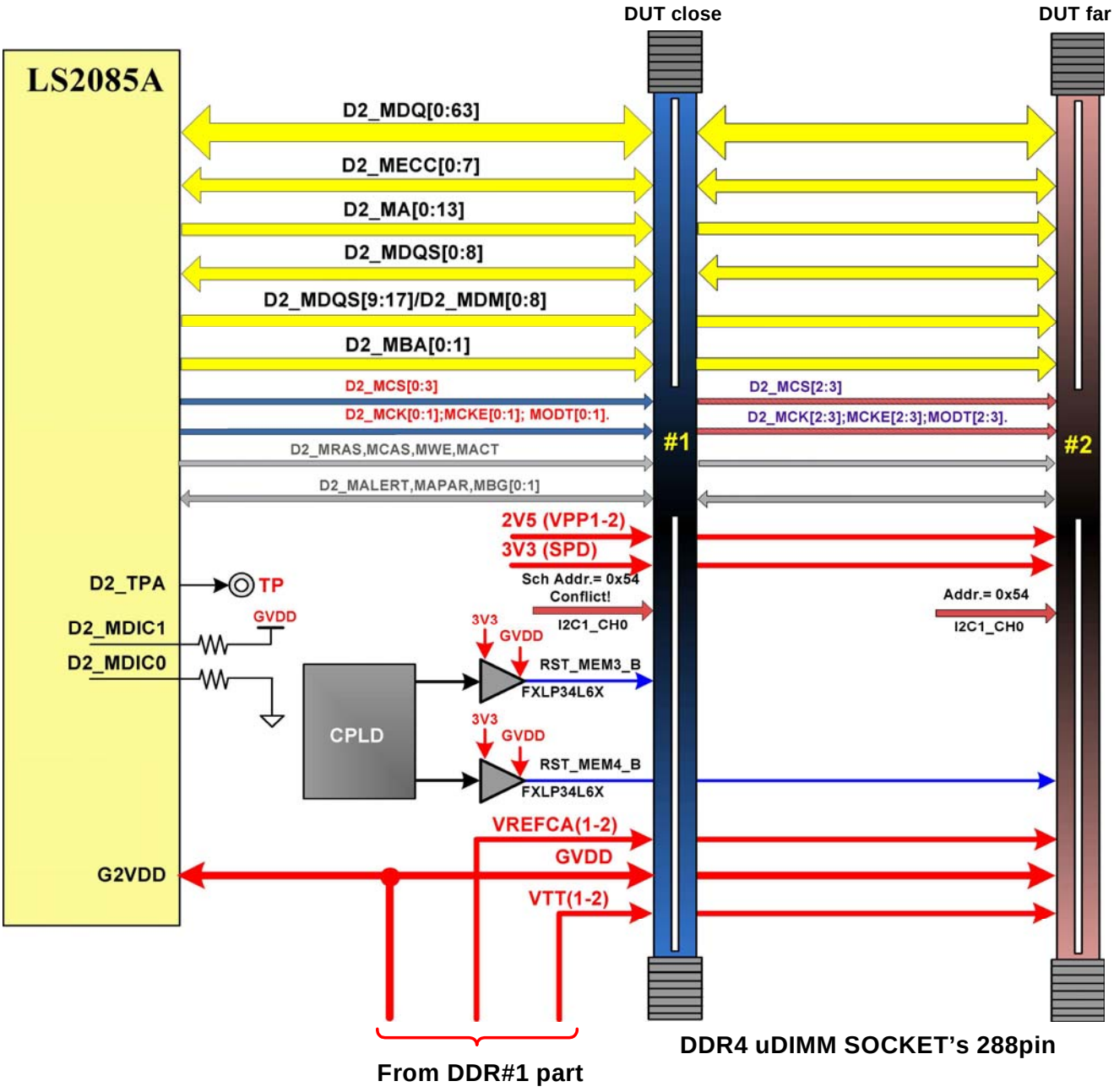


Figure 2-2. LS2085A RDB DDR Port D2 interface

Figure 2-3 shows DDR port D3 memory architecture.

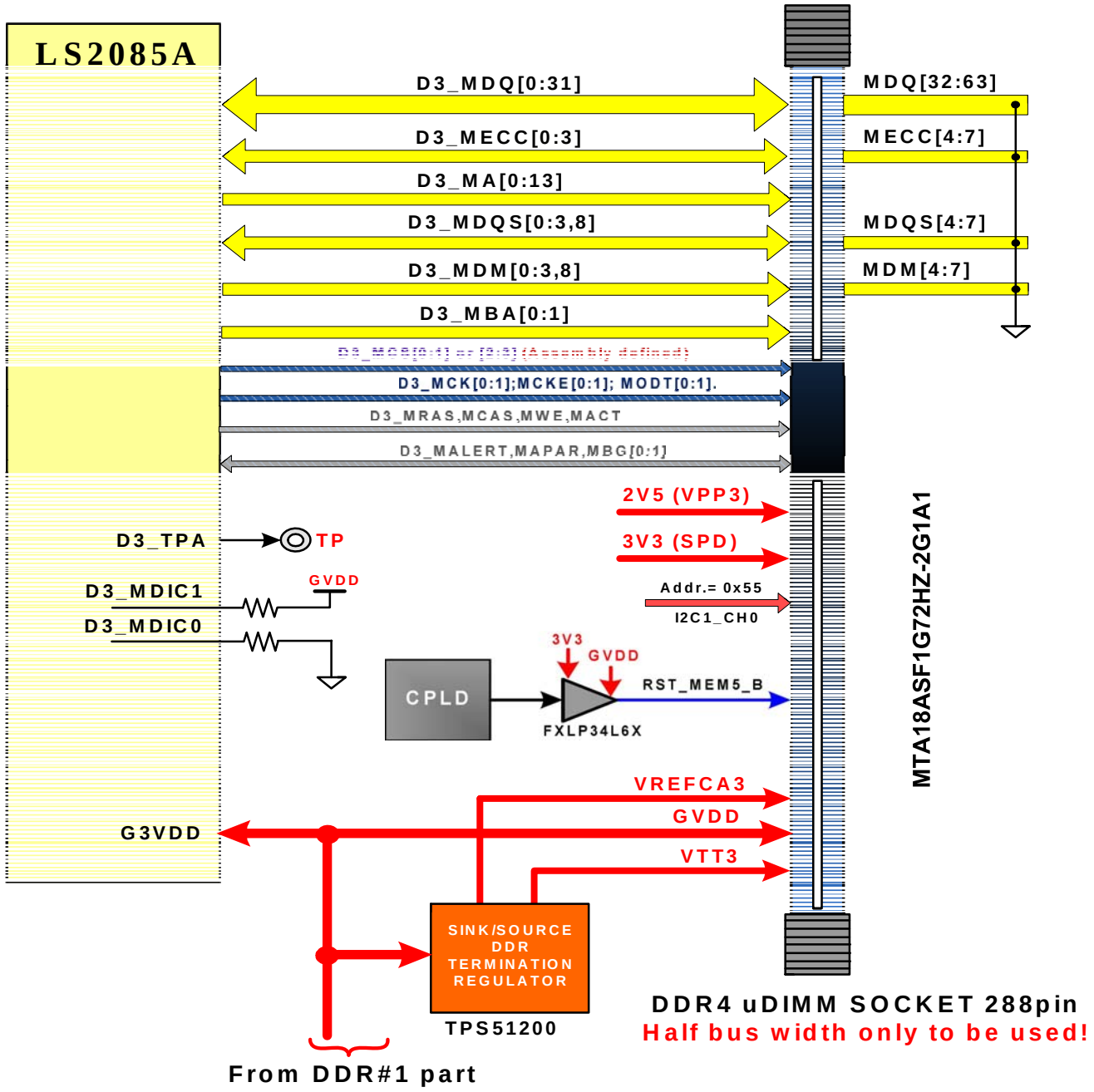


Figure 2-3. LS2085A RDB DDR Port D3 interface

2.1.1 DDR power

LS2085A RDB DDR power supply provides the following voltages for DDR4:

Table 2-1. DDR power supply

Voltage Name	Voltage	Current	NOTE
GVDD	1.2 V	<=10A	DRAM core and IO
MVREFCA(1-2)	0.6 V	>=10mA	DRAM ports D1 and D1 CA reference voltage
MVREFCA3	0.6 V	>=10mA	DRAM ports D3 CA reference voltage
VTT(1-2)	0.6 V	<=3A	ports D1 and D2 Bus termination supply
VTT3	0.6 V	<=3A	port D3 Bus termination supply

The LS2085A RDB uses the IR3565 (UP2) switching power controller as:

- Dual-phase #1 VDD up to 60 A at a default 1.0 V output for LS2085A core and platform.
- Single-phase #2 GVDD up to 30 A at a default 1.2 V output for LS2085A DDR controllers (GVDD all three ports) and all DIMM's GVDD supply (of all three ports).

One LDO voltage regulator (UP10) generates 50% of GVDD voltage as VREFCA(1-2) and VTT(1-2) for ports D1 and D2. A second LDO voltage regulator (UP9) generates 50% of GVDD voltage as VREFCA3 and VTT3 for port D3.

The use of MECC pins by LS2085A RDB can be summarized as follows:

- RDB does not directly support MECC pin usage to access internal debug information. Since the RDB does not provide a dedicated MUX, its has simpler routing and signal integrity status.
- However, as the RDB does not interfere with the controller-to-DDR path, access to debug information on MECC pins is possible by using a NextWave (or equivalent) DDR logic analyzer connector and non-ECC DDR modules.

2.1.2 DDR power setup

2.1.3 Compatible DDR4 modules

The LS2085A RDB DDR interfaces work with any JEDEC-compliant, 288-pin, DDR4 uDIMM modules.

Table 2-2 lists uDIMM modules that are tested and confirmed with the LS2085A DDR controller.

Table 2-2. DDR4 modules

Manufacturer	Part Number	Size	Ranks	ECC	Data Rate	Verified
Micron	MTA18ASF1G72AZ-2G1A1 (UDIMM)	8 GB	Dual Rank	Yes	2133 MT/s	V
Micron	MTA9ASF51272AZ-2G1A1 (UDIMM)	4 GB	Single Rank		2133 MT/s	V
Micron	MTA18ASF1G72HZ-2G1A1 (SODIMM)	8 GB	Dual Rank		2133 MT/s	V

2.2 SerDes (Serializer/Deserializer)

The LS2085A SerDes[1] block supports several protocols which includes 16 serial lanes[2] that are partitioned as 8 lanes for SERDES1 (SD1) and 8 lanes for SERDES2 (SD2). See *LS2085A Integrated Multicore Communication Processor Family Reference Manual* for information regarding supported SerDes combinations.

Table 2-3. LS2085A RDB SerDes embedded devices

Manufacturer	Part Number	Description
Foxconn	LE18077-Z54D-4H	Two vertical SATA connectors
Pericom	PI3PCIE3413ZHE	• Two differential channels, 3:1 MUX/DeMUX switch, PEX, Gen3, 8.0 Gbits/s compliance • Switch selects between four different Lynx Protocol Peripherals. • CPLD control SerDes2 MUX
ALL BEST ELECTRONICS	R-SS-008020-9-N	• Front port SFF 8431 (SFP+) optical and direct attach copper
ALL BEST ELECTRONICS	R-SH-008080-6-B-09	SUBASSEMBLY SFP+ CAGE 4 PORT PRESS-FIT RA TH
Source Photonics	SPP-10E-SR-CDFD	SFP+ Modules
WIN WIN Precision	WPES-064AN41B22UWS	• 1 x SMT, female, PEX x 4onboard slots • Supports PEX add-in cards
TECH BEST	1-80098-S501	• 1 x SMT, female, PEX x 8 onboard slots • Supports PEX add-in cards

Figure 2-4 and Figure 2-5 describes the possible SerDes 1 and 2 protocol combination for LS2085. The X on the right-side of each row indicates that that mapping shall not be supported by the RDB while the check mark indicates it can be supported.

1. The SerDes term describes a Serializer/Deserializer pair of functional blocks commonly used in HS communications to compensate for limited input/output. These blocks convert data between serial data and parallel interfaces in each direction.
2. Lane describes the minimum number of signals needed to create a bidirectional communication channel.

Figure 2-4. LS2085A SerDes 1 Protocol combination

LEFT SERDES								
SERDES PROTOCOL	OPTICAL PHY (CS4340, U58)				COPPER PHY (AQR405, U60)			
	0	1	2	3	4	5	6	7
0x2A	XFI1 (M S)	XFI2 (M S)	XFI3 (M S)	XFI4 (M S)	XFI5	XFI6	XFI7	XFI8

Figure 2-5. LS2085A SerDes 2 Protocol combination

	RIGHT SERDES							
SW6[3:4]=01	SERDES	SLOT #0 (CONNECTOR CN4)							
	PROTOCOL	0	1	2	3	4	5	6	7
	0x3D	PEX3[0]	PEX3[1]	PEX3[2]	PEX3[3]	PEX3[4]	PEX3[5]	PEX3[6]	PEX3[7]
	0x3E	PEX3[0]	PEX3[1]	PEX3[2]	PEX3[3]	PEX3[4]	PEX3[5]	PEX3[6]	PEX3[7]

	RIGHT SERDES							
SW6[3:4]=10	SERDES	SLOT #0 (CONNECTOR CN4)				SLOT #1 (CONNECTOR CON1)			
	PROTOCOL	0	1	2	3	4	5	6	7
	0x3F	PEX3[0]	PEX3[1]	PEX3[2]	PEX3[3]	PEX4[0]	PEX4[1]	PEX4[2]	PEX4[3]
	0x40	PEX3[0]	PEX3[1]	PEX3[2]	PEX3[3]	PEX4[0]	PEX4[1]	PEX4[2]	PEX4[3]
	0x41	PEX3[0]	PEX3[1]	PEX3[2]	PEX3[3]	PEX4[0]	PEX4[1]	~~SATA1~~	~~SATA2~~
	0x42	PEX3[0]	PEX3[1]	PEX3[2]	PEX3[3]	PEX4[0]	PEX4[1]	~~SATA1~~	~~SATA2~~

	RIGHT SERDES							
SW6[3:4]=11	SERDES	SLOT #0 (CONNECTOR CN4)						SATA CON2	SATA CON3
	PROTOCOL	0	1	2	3	4	5	6	7
	0x43	PEX3[0]	PEX3[1]	PEX3[2]	PEX3[3]	X	X	SATA1	SATA2
	0x44	PEX3[0]	PEX3[1]	PEX3[2]	PEX3[3]	X	X	SATA1	SATA2
	0x41	PEX3[0]	PEX3[1]	PEX3[2]	PEX3[3]	PEX4[0]	PEX4[1]	SATA1	SATA2
	0x42	PEX3[0]	PEX3[1]	PEX3[2]	PEX3[3]	PEX4[0]	PEX4[1]	SATA1	SATA2

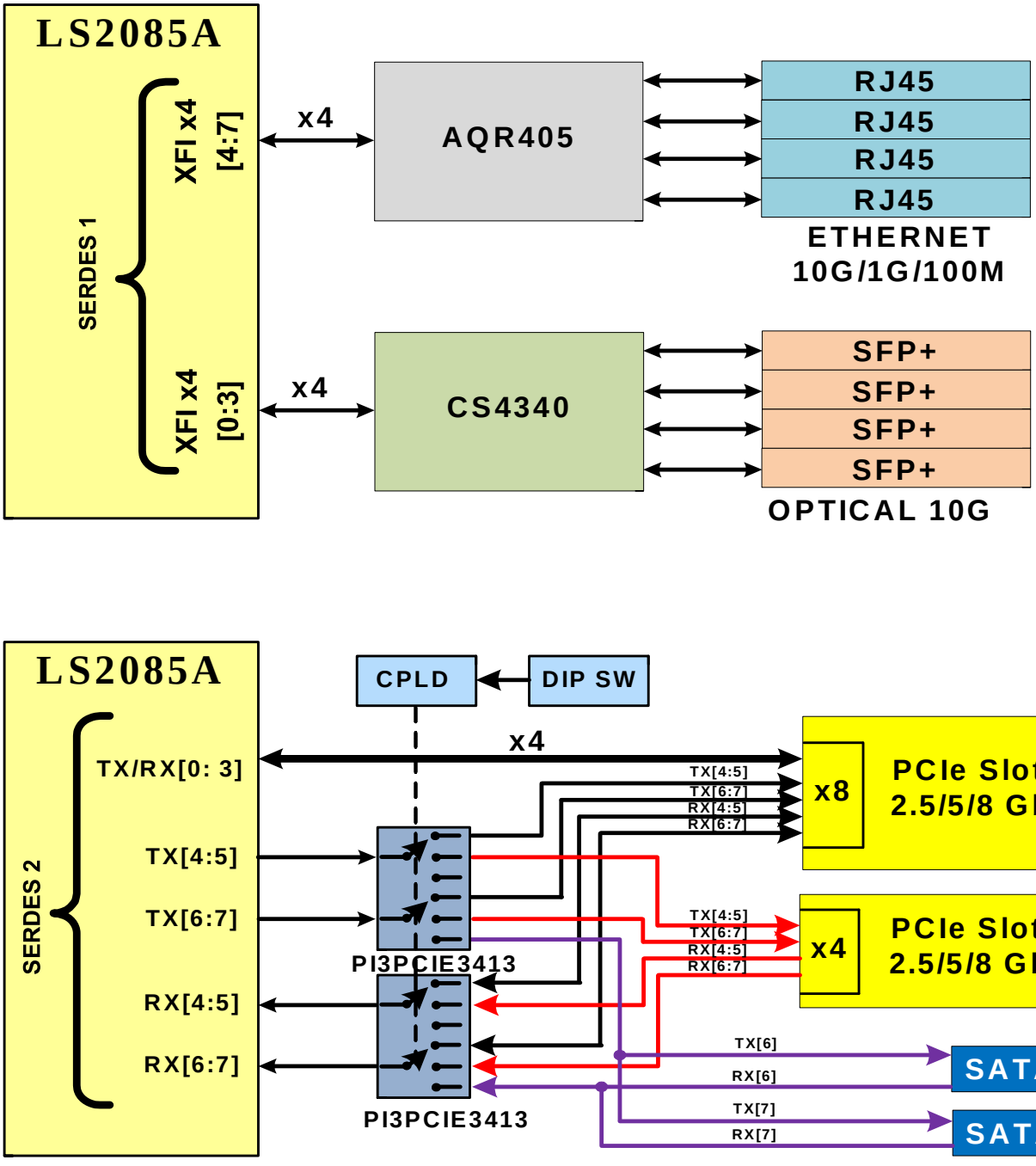


Figure 2-6. LS2085A RDB SerDes Lane connection

•

2.2.1 SerDes configuration and setup

The SerDes multiplexers can be configured with two DIP-switch bits SW6[3:4] that is connected to the CPLD. The CPLD will attempts to set the SerDes mux which is based on the DIP-switch values, which should be set to match the selected RCW[SRDS_PRTCL_Sn] field.

Table 2-4 below shows the mapping between the SerDes DIP-switch that controls the multiplexers appearing in Figure 2-6.

Table 2-4. LS2085A RDB SerDes mux configuration

PI3PCIE3413 SEL1	PI3PCIE3413 SEL2	SerDes Function Allowed	Note
0	0	Power down	
0	1	PCIe x8 on Slot x8	
1	0	PCIe x4 on Slot x8	
1	1	PCIe Slot x8 in x4 mode and two SATA 3.0 ports	

2.2.2 Front panel connection for SerDes

Looking at the RDB front panel, Figure 2-7 shows the location of where to plugin the CAT 6A or CAT 7 cable for copper connection and fiber cable for optical connection. CAT 6A and CAT 7 cable will allow signal to go for 100m with no significant degration. CAT 6 is only good for 55m. The picture also shows what XFI number is connected to which port.

Figure 2-8 shows the location of SATA connectors on the board and the reference designators.

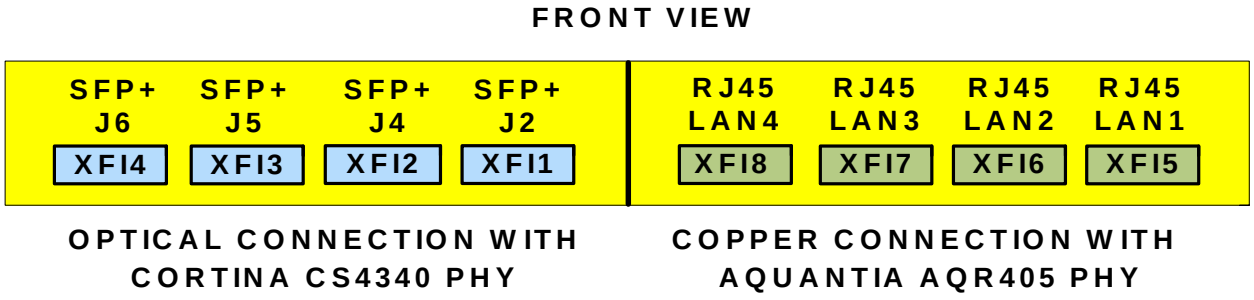


Figure 2-7. Optical and Copper connection

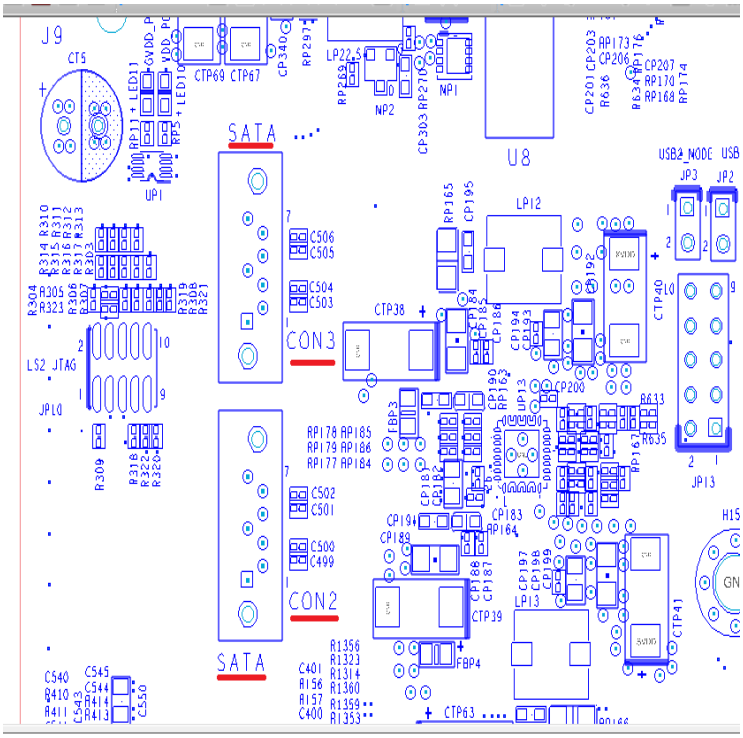


Figure 2-8. SATA connectors

2.3 Ethernet (ETH) controller interface

The LS2085A does not support independent ETH controllers. ETH connections are only available over SerDes interfaces 1 and 2 (SGMII, SGMII2.5, QSGMII, XFI, XAUI). On the RDB, 10 Gbps, 1 Gbps and 100 Mbps Ethernet will be supported on SerDes 1 from lanes 4 to 7. The XFI is supported on SerDes 1 lanes 0 to 3. SerDes 2 is chosen to support SATA and PCIe since they are coexist in that controller.

2.3.1 Support for IEEE 1588™ PTP standard protocol

The LS2085A includes support for the IEEE 1588™ Precision Time Protocol (PTP) and works in tandem with the ETH controller to time-stamp the incoming packets. A 12-pin header JP4 is provided on the RDB to allow support of 1588 protocol.

Figure 2-9 shows the organization of the IEEE 1588 system.

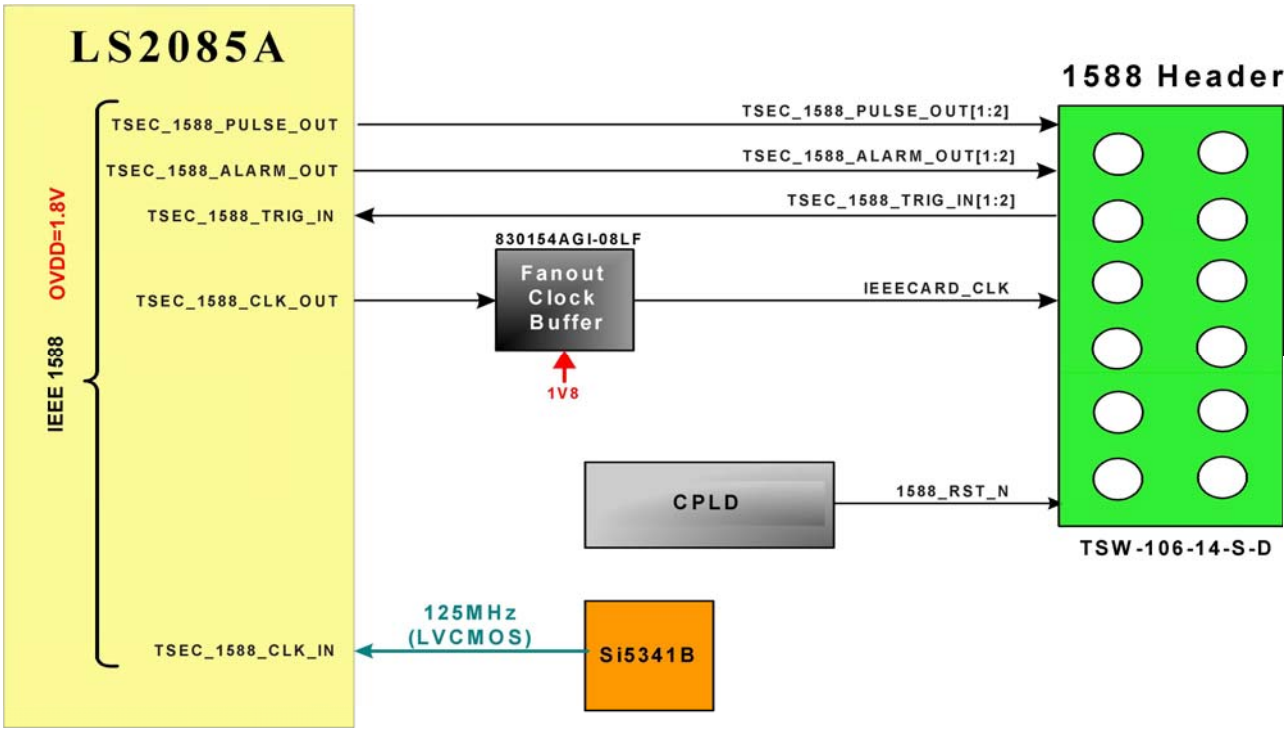


Figure 2-9. LS2085A RDB IEEE 1588 interface

The 1588 Test Header provides testing options.

Table 2-5. IEEE 1588™ port

IEEE1588™ Feature	Specifics	Description
IEEE 1588™ Clocks	Input clock	Input clock is driven from a 125 Mhz oscillator sources.
	Output clock	Output clock is driven to a 1588 header using IDT 83015AGI-0LF fanout clock buffer.
IEEE 1588™ signals	Other related signals	All remaining LS2085A IEEE 1588™ signals are connected to the 1588 header.

2.3.2 MII management buses

The LS2085A has two MII buses to control two separate PHY transceiver devices. The two buses (EMI1 and EMI2) are connected to the Cortina CS4340 PHY and the Aquantia AQR405 PHY. Figure 2-10 shows the PHY device connection to the management buses. Both device has four internal PHYs. Table 2-6 shows the address to access the internal PHY on both devices.

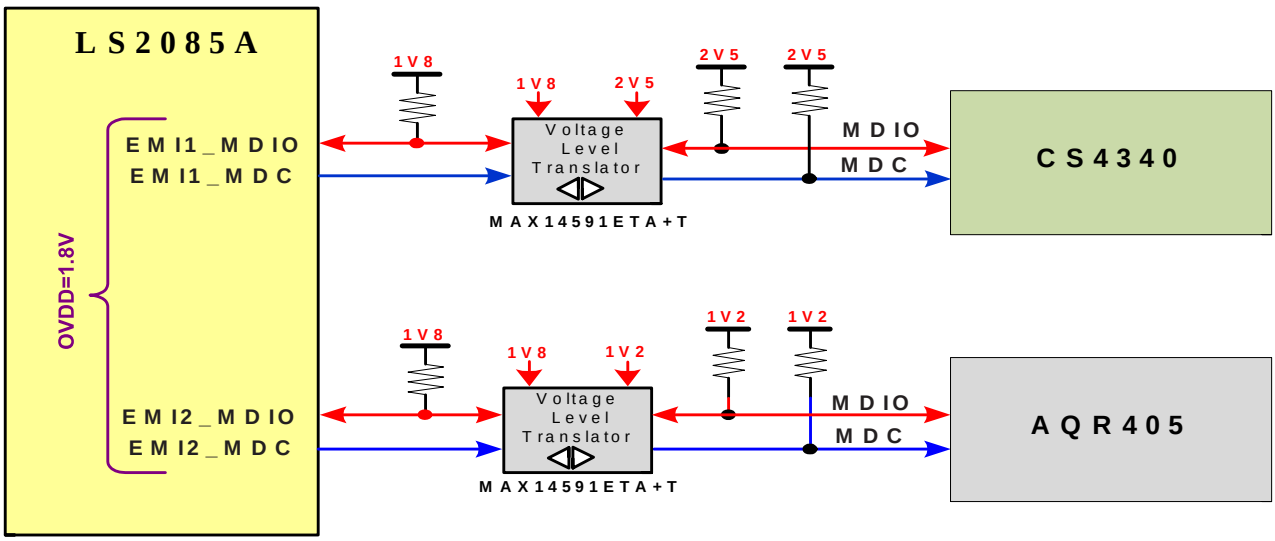


Figure 2-10. MII management buses

Table 2-6. EMI PHY Address

Device	Internal PHY number	Address [4:0]
AQUANTIA AQR405 U60	1	0x00
AQUANTIA AQR405 U60	2	0x01
AQUANTIA AQR405 U60	3	0x02
AQUANTIA AQR405 U60	4	0x03
CORTINA CS4340 U58	1	0x10
CORTINA CS4340 U58	2	0x11
CORTINA CS4340 U58	3	0x12
CORTINA CS4340 U58	4	0x13

2.4 Integrated Flash Controller (IFC)

The IFC has the following features:

- New IFC revision 2.0
- Implements Little Endian support
- Supports 27-bit addressing and 8-/16-bit data bus
- Supports GPCM, NOR and NAND FCM
- 1.8V IO voltage
- Supports the following IFC clients on LS2085A RDB:
  - NAND flash (Async/sync - ONFI 2.2 compatible)
  - NOR flash 16-bit

Figure 2-11 shows the IFC block diagram.

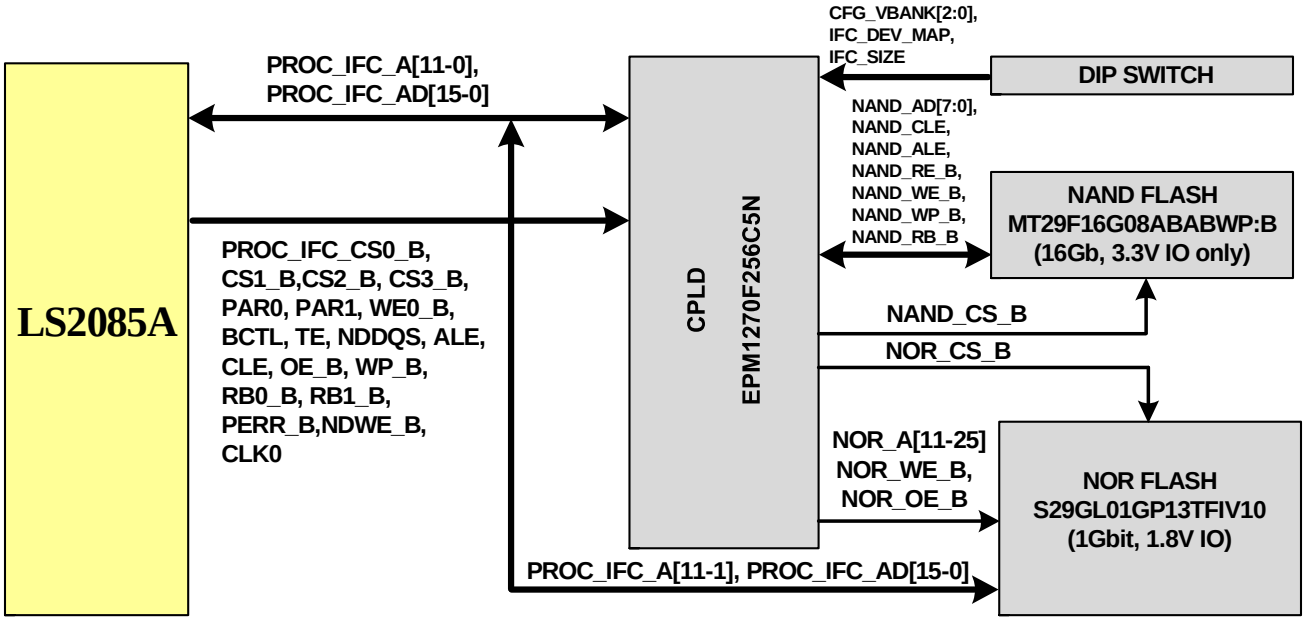


Figure 2-11. IFC interface

LS2085A RDB uses a combination of the IFC chip select signals and DIP Switch SW6[1:2] and SW9[1:3] called IFC_DEV_MAP, IFC_SIZE, SW_CFG_VBANK[0:2] to allow dynamic reconfiguration of the IFC boot device (which addressed the IFC_CS_B[0] only).

Table 2-7 summarizes IFC chip select routing.

Table 2-7. IFC chip select device mapping

SWx_LBMAP[0] = CFG_LBMAP[0]	CS#	Memory	Address	Data Width	
0	CS0	NOR Flash	TBD	16 bits	
	CS1	NAND Flash	TBD	8 bits	
	CS2	CPLD Registers	TBD	8 bits	
1	CS0	NAND Flash	TBD	8 bits	
	CS1	NOR Flash	TBD	16 bits	
	CS2	CPLD Registers	TBD	8 bits	

2.4.1 NOR flash

The NOR Flash device is the Spansion NOR flash memory (S29GL01GP13TFIV10) whis is a 128 MB memory with 8/16-bit data bus. This device is powered with 3.3V but the signals are driven with 1.8V IO level. The flash is controlled by the NOR IFC machine.

Flash controls are detailed below:

- IFC OE_B controls FLASH OE, while IFC WE0_B controls the FLASH $\overline{\text{WE}}$ signal.
- FLASH RY/$\overline{\text{BY}}$ output signal show the ready/busy status of the flash. This signal is connected to the CPLD.
- IFC_NOR_CS_B driven by CPLD selects NOR flash depending on CFG_Vbank[0...2].
- CPLD-generated signals are used to re-arrange internal addresses as per user configuration options CFG_LBMAP[0] (see Table 2-7)

2.4.2 NAND Flash

The ONFI 2.2 compatible Micron NAND flash memory (MT29F16G08ABABAWP:B) with 2 GB size and 8-bit data is assembled on the board. This is a 3.3V device and signals going to and from the LS2085A is buffered by the CPLD since the NAND only uses 3.3V IO signals. NAND flash is controlled by the LS2085A IFC FCM machine.

- FLASH R/$\overline{\text{B}}$ output indicates the status of a the NAND operation. This open drain output connects to the CPLD.
- IFC_NAND_CS_B from CPLD drives the NAND flash as per CFG_LBMAP[0], see Table 2-7.

2.5 Clocks

Figure 2-12 shows the LS2085A RDB clocking scheme and Table 2-8 summarizes the LS2085A RDB clock distribution.

NOTE

Historically, for the RDB, we do not support Spread Spectrum for SerDes clocking.

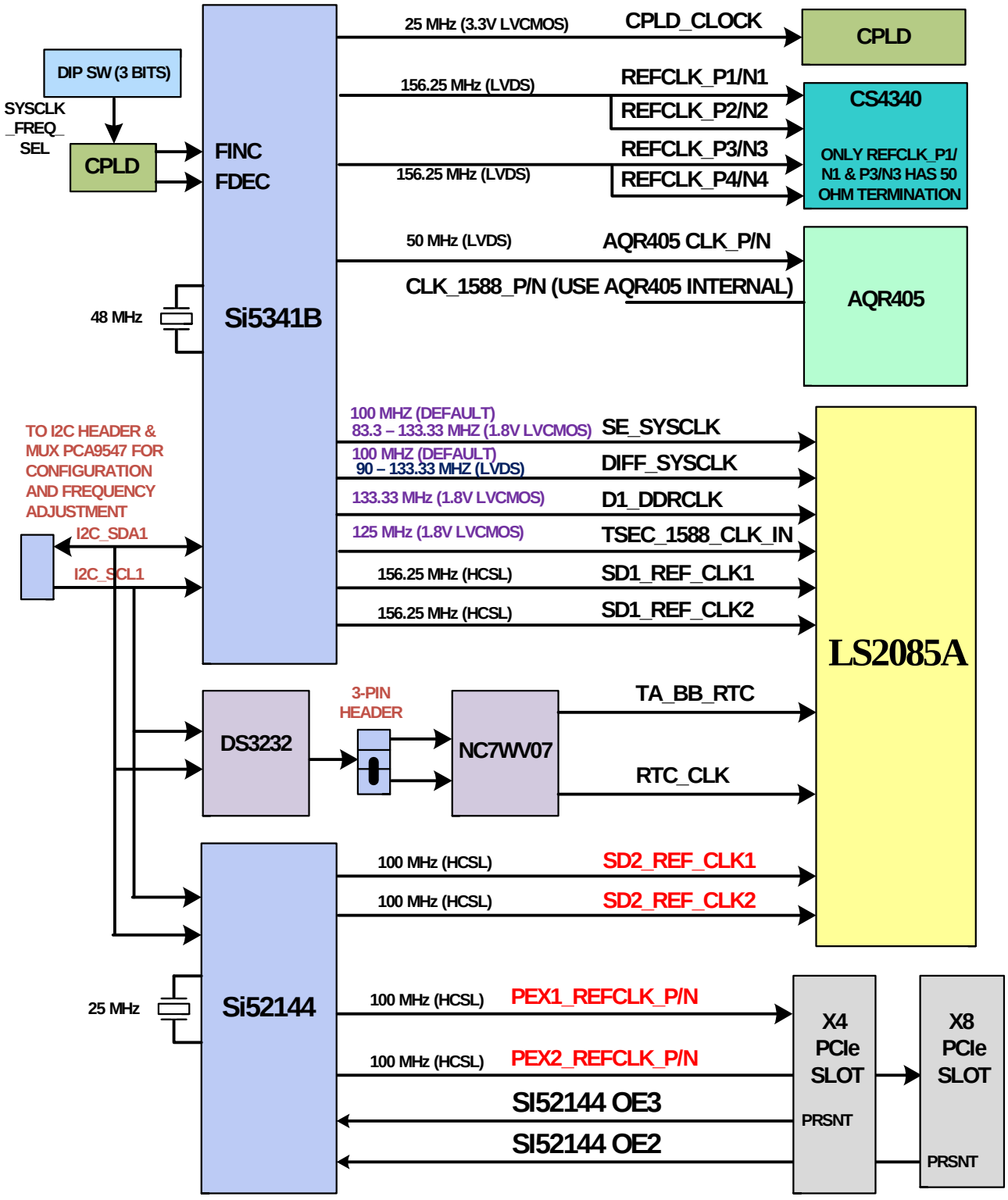


Figure 2-12. Clocking scheme

Table 2-8. LS2085A RDB clocks

Clock	Frequency	Destination	Device
SI5341B SE_SYSCLK	100 MHz (1.8V LVCMOS)	LS2085A SYSCLK	Si5341B: • Generate free-running or synchronous output clocks. • MultiSynth technology enables any-frequency synthesis on any-output with 0 ppm frequency accuracy • LVDS, LVPECL, LVCMOS, HCSL output drivers • 250 fs RMS typical jitter • External crystal input: 25, 48-54 MHz • Differential output range: 1 kHz to 800 MHz • LVCMOS output range: 1 kHz to 250 MHz • Output-output skew: < 100ps • Adjustable output-output delay: 65536 steps, 1ps/step • Independent glitchless on-the-fly output frequency changes • Frequency increment and decrement as low as 0.01 ppb/step • Vdd core voltage: 1.8V +/-5% • Vdda core voltage: 3.3V +/-5% • Built-in power supply filtering • LOS, LOL status monitoring • I2C or SPI serial interface
SI5341B DIFF_SYSCLK_P/N	100 MHz (LVDS)	LS2085A DIFF_SYSCLK	
SI5341B D1_DDRCLK	133.3 MHz (1.8V LVCMOS)	LS2085A D1_DDRCLK	
SI5341B SD1_REF_CLK1_P/N SD1_REF_CLK2_P/N	156.25 MHz (LVDS)	LS2085A SD1_REF_CLK1 SD1_REF_CLK2	
SI5341B TSEC_1588_CLK_IN	125 MHz (1.8V LVCMOS)	LS2085A TSEC_1588_CLK_IN	
OSCILLATOR CPLD_CLK	25 MHz (3.3V LVCMOS)	CPLD	
CLK_P/N	50 MHz (LVDS)	AQR405 CLK_P/N	
SI5341B CS4340_REFCLK_1_2_P/N, CS4340_REFCLK_3_4_P/N	156.25 MHz (LVDS)	CS4340 Ethernet PHY: REFCLK_P1/N1 REFCLK_P2/N2 REFCLK_P3/N3 REFCLK_P4/N4	
	50 MHz	AQR405 PHY CLK_1588_P/N	USE ONCHIP INTERNAL AQR405 CLOCK. DERIVED FROM CLK_P/N
SI52144 SD2_REF_CLK1_P/N SD2_REF_CLK2_P/N	100 MHz (HCSL)	LS2085A SD2_REF_CLK1 SD2_REF_CLK2	Si52144: • Four PCIe Gen1, Gen2 & Gen3 clocks • Supports SATA at 100 MHz • Low power, push pull HCSL diff outputs • No termination required • Output enable pn for each output • Hardware pin for spread spectrum control • 25 MHz crystal or clock input • I2C support with readback
SI52144 PEX1_REFCLK_P/N	100 MHz (HCSL)	PEX X4 SLOT #1 PEX1_REFCLK_P/N	
SI52144 PEX2_REFCLK_P/N	100 MHz (HCSL)	PEX X8 SLOT #2 PEX2_REFCLK_P/N	
RTC	32 kHz	LS2085A: RTC_CLK OR TA_BB_RTC	DS3232
TSEC_1588_ CLKOUT	125 MHz	1588 Test Connector	IDT 830154AGI-08LF • LOW SKEW, 1-TO-4 LVCMOS Fanout buffer with output disable • Max output frequency =160MHz • t_r / t_f <= 1.2ns • Duty-cycle <=60%
			•

2.5.1 Clocks frequency configuration

The Silicon Labs Si5339B device come with default frequency value preconfigured. Only the SYSCLK frequency can be changed with a DIP switch SW7[1:3]. See Table 2-9 on the frequency selection. If the frequency value needs to be updated on the Si5241B for SYSCLK, DDRCLK, SD1_REF_CLK1, DIFF_SYSCLK, TSEC_1588_CLK, USB_CLKIN, AQR405_CLK or CS4340_REFCLK_1_2, then the I2C header and the Silicon Lab ClockBuilder Pro software utility can be utilised for that to happen.

Table 2-9. Switch SW7[1:3] SYSCLK frequency selection

SEL2	SEL1	SEL0	SELECTED SYSCLK FREQUENCY
0	0	0	66.666667 MHZ
0	0	1	83.333333 MHZ
0	1	0	100.000000 MHZ
0	1	1	125.000000 MHZ
1	0	0	133.333333 MHZ
1	0	1	150.000000 MHZ
1	1	0	160.000000 MHZ
1	1	1	166.666667 MHZ

2.6 Serial interfaces

LS2085A has several serial interfaces including RS232, eSPI, eSDHC/eMMC and I2C.

2.6.1 UART serial ports

Figure 2-13 shows the LS2085A UART connections.

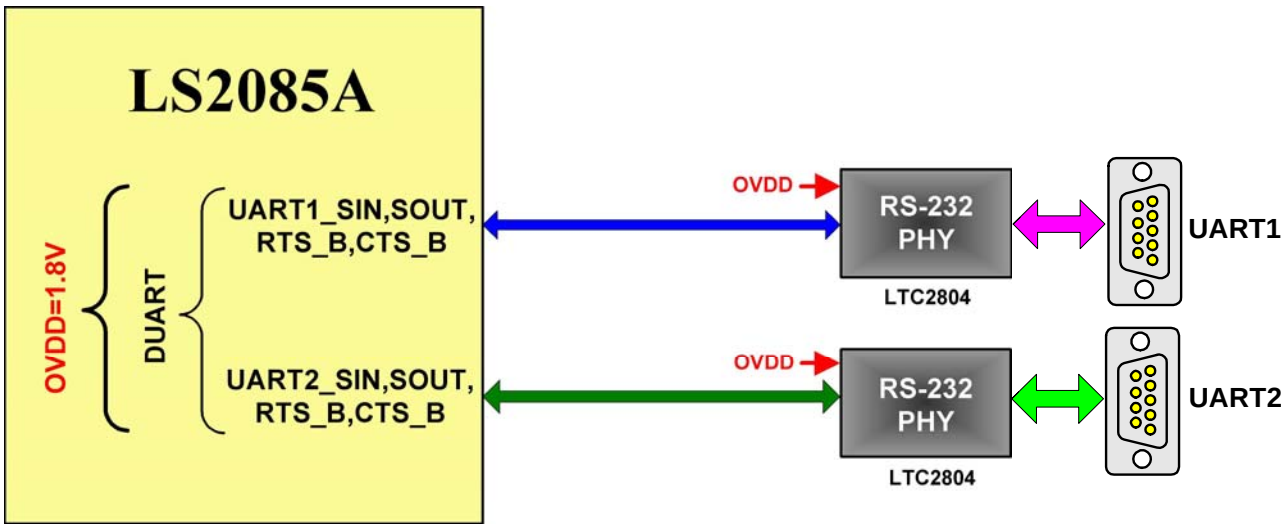


Figure 2-13. UART interface

The LS2085A has two full UART ports (with HW flow control) or four UART ports with no flow control. On the board there are two UART connectors so two ports can be available at a time. Two RS-232 transceivers from Linear Technology (LTC2804-1) on the LS2085A RDB contribute to user application development and provide convenient communication channels to both terminal and host computers. The transceivers are connected to LS2085A dedicated UART ports by 4 wires including RTS/CTS flow control using level shifters from OVDD to 3V3HOT voltage.

Table 2-10 describes the LS2085A RDB RS-232 interface.

Table 2-10. LS2085A RDB RS232 interface

UART Ports	Destination	Power supply	Flow control	External Connector
UART1	Terminal (Host Computer)	3.3V	Supported	UART1/3 (P1 Bottom)
UART3			Unsupported	
UART2			Supported	UART2/4 (P1 Top)
UART4			Unsupported	

2.6.2 enhanced Serial Peripheral Interface (eSPI)

Figure 2-14 shows the LS2085A connections for eSPI and SD memory.

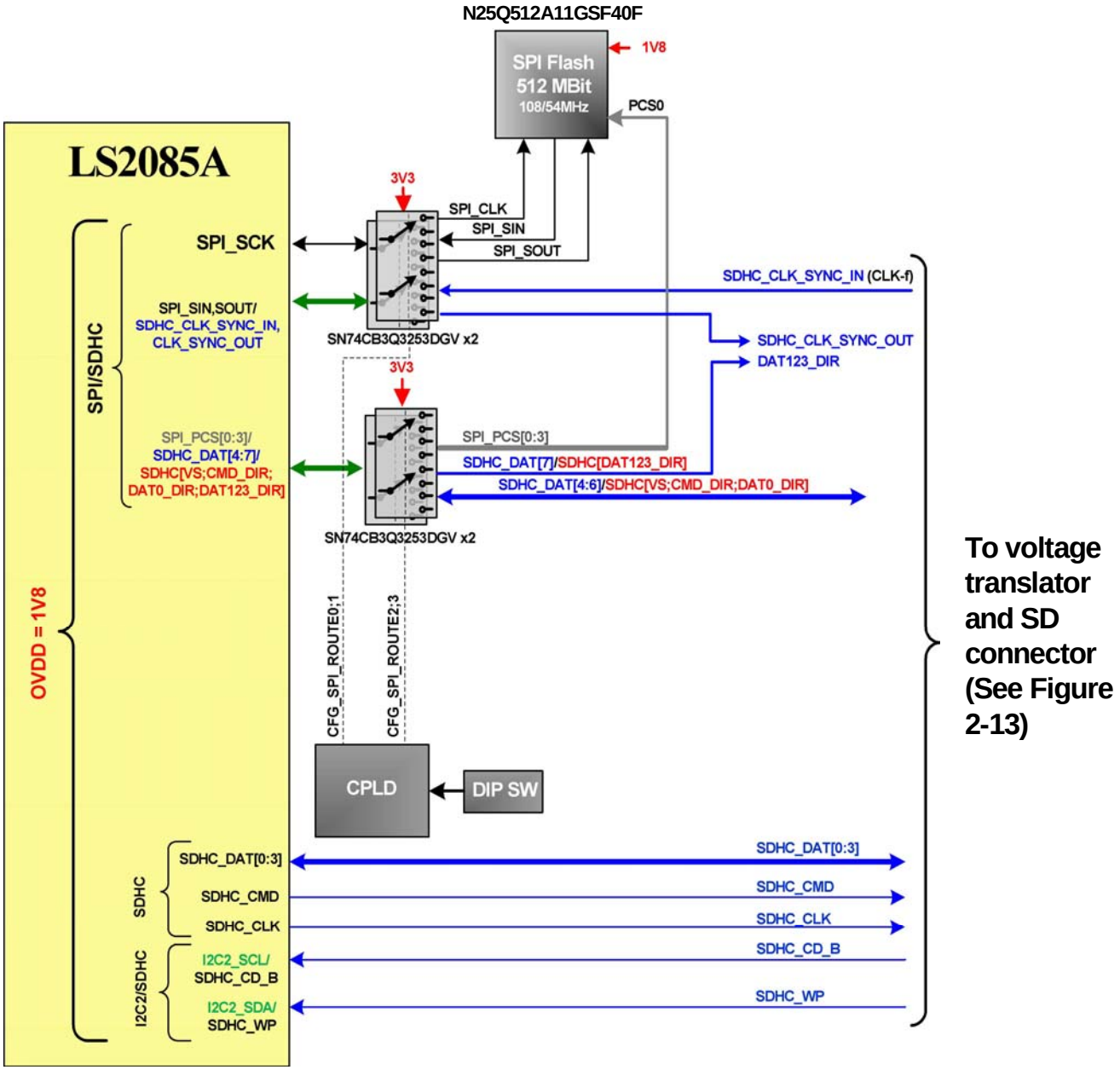


Figure 2-14. eSPI and eSDHC connections

NOTE

Some eSPI pins are muxed with eSDHC pins so eSPI functionality depends on eSDHC configuration.

The LS2085A has an eSPI Master Controller that is used to communicate with various peripherals.

- SPI flash memories support 32-bit address and SPI Modes 0, 3.
- LS2085A OVDD supports 1.8 V on LS2085A RDB.
- LS2085A SPI_CS[0:3] are muxed with LS2085A SDHC_DAT[4:7]. Muxes are used on board.
- Chip Select 1, 2 and 3 are not used.

Table 2-11 describes LS2085A RDB SPI flash memory.

Table 2-11. eSPI slave devices

Device	Clock Frequency (MHz)	Voltage Range (V)	Capacity	SPI CS
Micron N25Q512A11GSF40F	108	1.7-2.0V	64 MB	CS0

2.6.2.1 SPI configuration and setup

The SPI routing configuration is described in the following table.

Table 2-12. SPI configuration

Configuration Signal	Control	Value	Description
CFG_SPI_ROUTE[0:3] (from CPLD)	TBD	0000	SD card 1-/4-bit access. No access to SPI memory N25Q512A11GSF40F. The following signals goes to SD card connector CN3 through level translator U36 (ST6G3244MEBJR). Through demux: SDHC_CLK_SYNC_IN SDHC_VS SDHC_CMD_DIR SDHC_DAT0_DIR SDHC_DAT123_DIR From LS2085: SDHC_DAT[0:3] SDHC_CMD SDHC_CLK SDHC_CD_B SDHC_WP
		0101	Access SPI memory N25Q512A11GSF40F. SPI CS0 memory is in use. No access for SD card.
		1010, 1111	Reserved

2.6.3 Enhanced Secure Digital Host Controller (eSDHC)

Figure 2-14 shows the LS2085A eSDHC connections.

The LS2085A supports 1-/4-bit SD/SDIO Rev 2.0 and 3.0. It has a level translator and a SD connector to support both SD card. Figure 2-15 shows the eSDHC signal connections supported on the RDB.

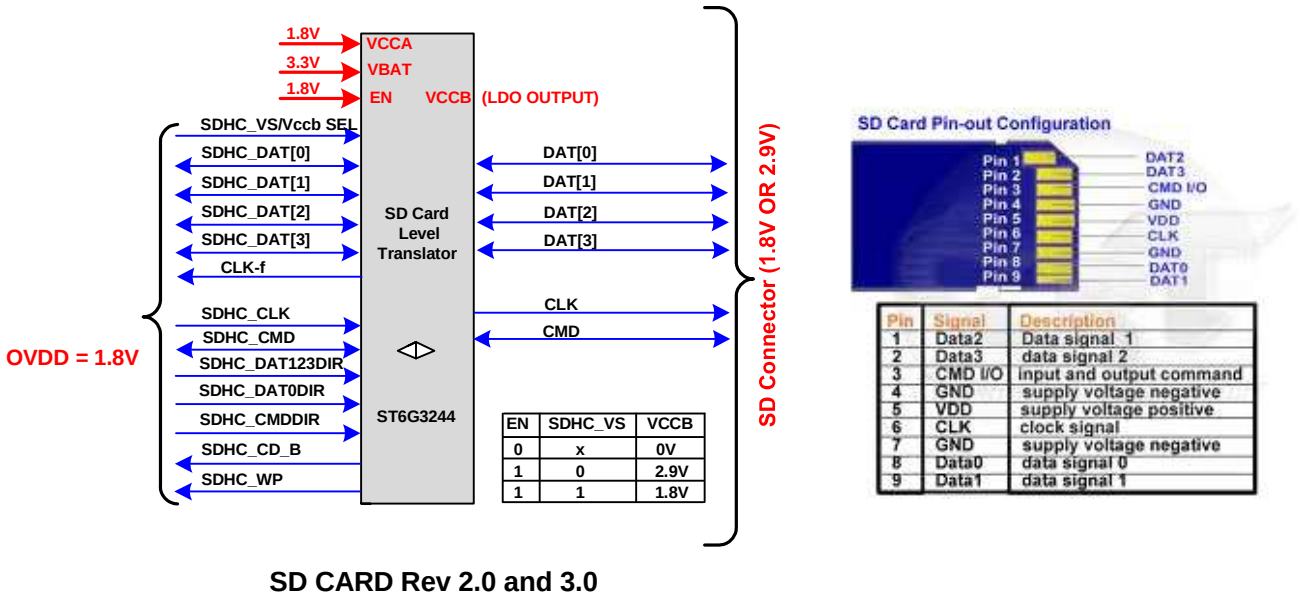


Figure 2-15. eSDHC connector

- x1/x4-bit SD Card supports SD Rev 2.0 and 3.0
  - LS2085A SDHC_VS(IRQ3) output signal is used to select between 1.8V/3.3 V SD card IO voltages . This signal is driven to a level translator device ST6G3244 from STMicroelectronics.
  - Special direction control pins are used. They are called LS2085A SDHC_CMD_DIR, SDHC_DAT0_DIR and SDHC_DAT123_DIR.
  - ST6G3244 CLK feedback is routed to SDHC_CLK_SYNC_IN for PCB routing delay compensation.

2.7 I^2C ports

The LS2085A has four I^2C buses:

- LS2085A I^2C1 is attached to all local devices on LS2085A RDB.
- Multiplexers are used to partition the I^2C1 bus into several sub-buses, called **channels**. All boot-software-dependent devices are placed on channel 0, called I^2C1_CH0. Channel 0 is selected by default on reset, so the software has immediate access to the critical resources.
- LS2085A I^2C2, I^2C3, are being reserved for board-to-board communications, or for user-purposes.
- LS2085A I^2C2 and I^2C4 are not used.
- External level shifter devices from NXP, called: PCA9517ADP are used on LS2085A I^2C1 and I^2C3.

Table 2-13 summarizes I^{2}C bus device addresses, while Figure 2-16 shows overall I^{2}C scheme connections.

Table 2-13. I^{2}C bus device map[1]

I^{2}C **Bus**	I^{2}C **Address**	**Device**	**Notes**
1-4	n/a	LS2085A	LS2085A I^{2}C Master on all buses
I^{2}C1	n/a	I^{2}C1_Remote system Header JP5	I^{2}C Master to access LS2085, DDR slots, EEPROM, RTC, clock generators, CORE & GVDD regulator, OVDD regulator, thermal monitor
I^{2}C3	n/a	I^{2}C1_Remote system Header JP9	I^{2}C Master to access LS2085, XFI 1, XFI 2, XFI 3, XFI 4, PCIe x4 slot, PCIe x8 slot
I^{2}C1	0x77	PCA9547PW	I^{2}C Bus multiplexer - First Tier Mux
I^{2}C3	0x75	PCA9547PW	I^{2}C Bus multiplexer - First Tier Mux
I^{2}C1_CH0	0x50	Atmel AT24C512C-XHM-T 512 KBit RCW EEPROM	• Stores RCW and Pre-boot loader data. • Write Protect (WP)
	0x57	Atmel AT24C02D-SSHM-T 2048 Bits EEPROM	• Store System ID
	0x51 0x52	Atmel AT24C02C 256 bytes EEPROM	• SPD EEPROM DDR port 1 DIMM#1 (U4) and DIMM#2 (U5) • Type of device depends on uDIMM vendor.
		Microchip MCP98242 (If any)	Thermal monitor may be present on uDIMM as well.
	0x53 0x54	Atmel AT24C02C 256 bytes EEPROM	• SPD EEPROM DDR port 2 DIMM#1 (U6) and DIMM#2 (U7) • Type of device depends on uDIMM vendor.
		Microchip MCP98242 (If any)	Thermal monitor may be present on uDIMM as well.
	0x55	Atmel AT24C02C 256 bytes EEPROM	• SPD EEPROM DDR port 3 DIMM#1 (U8) • Type of device depends on uDIMM vendor.
		Microchip MCP98242 (If any)	Thermal monitor may be present on uDIMM as well.
I^{2}C1_CH1	0x60	Si5341B	SE_SYSCLK, DIFF_SYSCLK
	0x61	Si52144	SD2_REF_CLK1,2_P/N
	0x68	DS3232: RTC	Used by software.

Table 2-13. I²C bus device map[1] (continued)

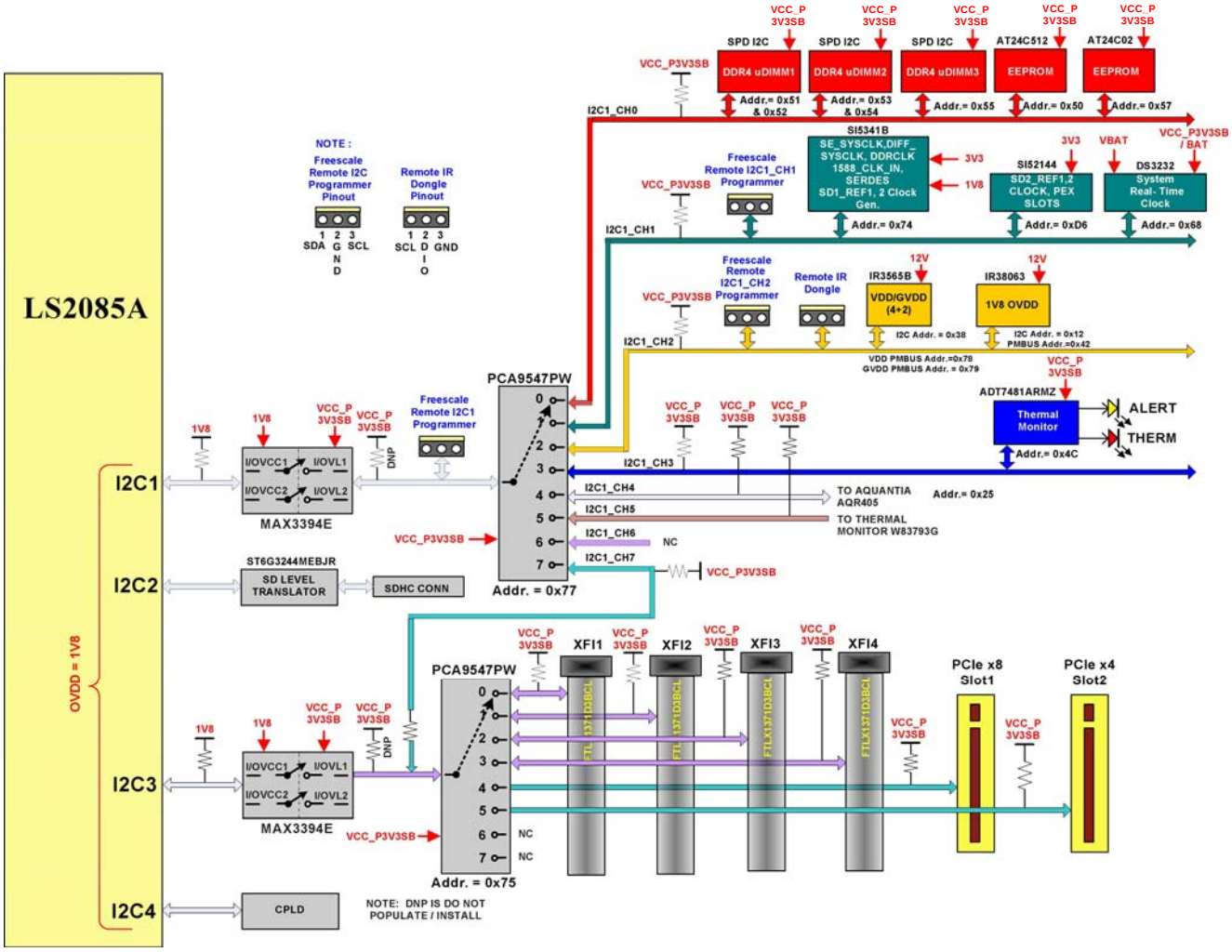
I²C Bus	I²C Address	Device	Notes
I²C1_CH2	0x38 0x78 0x79	International Rectifier IR3565B: • I²C Addr: 0x38 (7-bit addr) • VDD PMBus Addr :0x78 (7-bit addr) • GVDD PMBus Addr: 0x79 (7-bit addr)	Controls rails VDD (Core) and GVDD (DDR).
	n/a	I²C1_CH2 Access Header • Software team use JP7 • IR vendor use JP17	For remote programming of IR36021 Power Controller. Supports 3.3 V.
	0x12 0x42	International Rectifier IR38063: • I²C Addr: 0x12(7-bit addr) • PMBus Addr.0x42 (7-bit addr)	Controls rail OVDD
I²C1_CH3	0x4C	On Semiconductor ADT7481ARMZ Temperature Monitor	Monitors LS2085A Die Temperature
I²C2_CH3	0x75	PCA9547PW	I²C Bus multiplexer for XFI - Second Tier Mux
	0x75 (DUT) or 0x77 (CH7)+ CH0	10G Optical module	SFP_Module #1
	0x75 (DUT) or 0x77 (CH7)+ CH1	10G Optical module	SFP_Module #2
	0x75 (DUT) or 0x77 (CH7)+ CH2	10G Optical module	SFP_Module #3
	0x75 (DUT) or 0x77 (CH7)+ CH3	10G Optical module	SFP_Module #4
	0x75 (DUT) or 0x77 (CH7) +CH0+Slot1 Addr[2]	PEX Slot 1	I²C Address defined by PEX Slot 1 plugged-in Riser Card
	0x75 (DUT) or 0x77 (CH7) +CH0+Slot2 Addr[3]	PEX Slot 2	I²C Address defined by PEX Slot 2 plugged-in Riser Card
I²C2_CH4	0x25	AQUANTIA AQR405 10GE PHY 4 PORT Use JP14 (different pinout header) for debug	10 GE PHY
I²C2_CH5	0x5E 0x96 0x9E	WINBOND W83793G H/W MONITORING IC	SM Bus Address Temperature Sensor 1 Temperature Sensor 2

1 7-bit addresses do not include the R/W bit as an address member, though some datasheets might do so. For consistency, all I2C addresses are 7-bit of address only.

2 Access to the PEX slot I2C Devices requires programming the primary I2C mux at address 0x77, then the secondary I2C mux at address 0x75, then the specific plugged-in riser card address.

3 Access to the PEX slot I2C Devices requires programming the primary I2C mux at address 0x77, then the secondary I2C mux at address 0x75, then the specific plugged-in riser card address.

Figure 2-16. I2C scheme



2.8 Temperature anode and cathode

The LS2085A has four pins, TD1_Anode, TD1_Cathode, TD2_Anode and TD2_Cathode. All the pins are connected to a thermal body diode on the die that allows the direct temperature measurement. The pins are connected to an ADT7481 (U24) with dual channel thermal monitor that allows direct die temperature readings with an accuracy of ±1 °C.

In addition to triggering the software interrupts upon thermal problems, the ADT7481 temperature warning and alarm signals are used to drive indicators and are connected to the CPLD for monitoring. CPLD uses these signals to power down the system to protect the LS2085A from over-temperature failure.

2.8.1 Thermal configuration and setup

Thermal monitoring happens automatically with no programming involved. The ADT7481 defaults to a thermal limit of 85^0C. Thermal shutdown can be disabled by the configuration switch.

Table 2-14. Thermal monitor Configuration

Configuration Signal	Control	Value	Description
SW_BYPASS_B	TBD	0	Thermal shutdown prevented
		1	Thermal shutdown allowed (Normal mode)

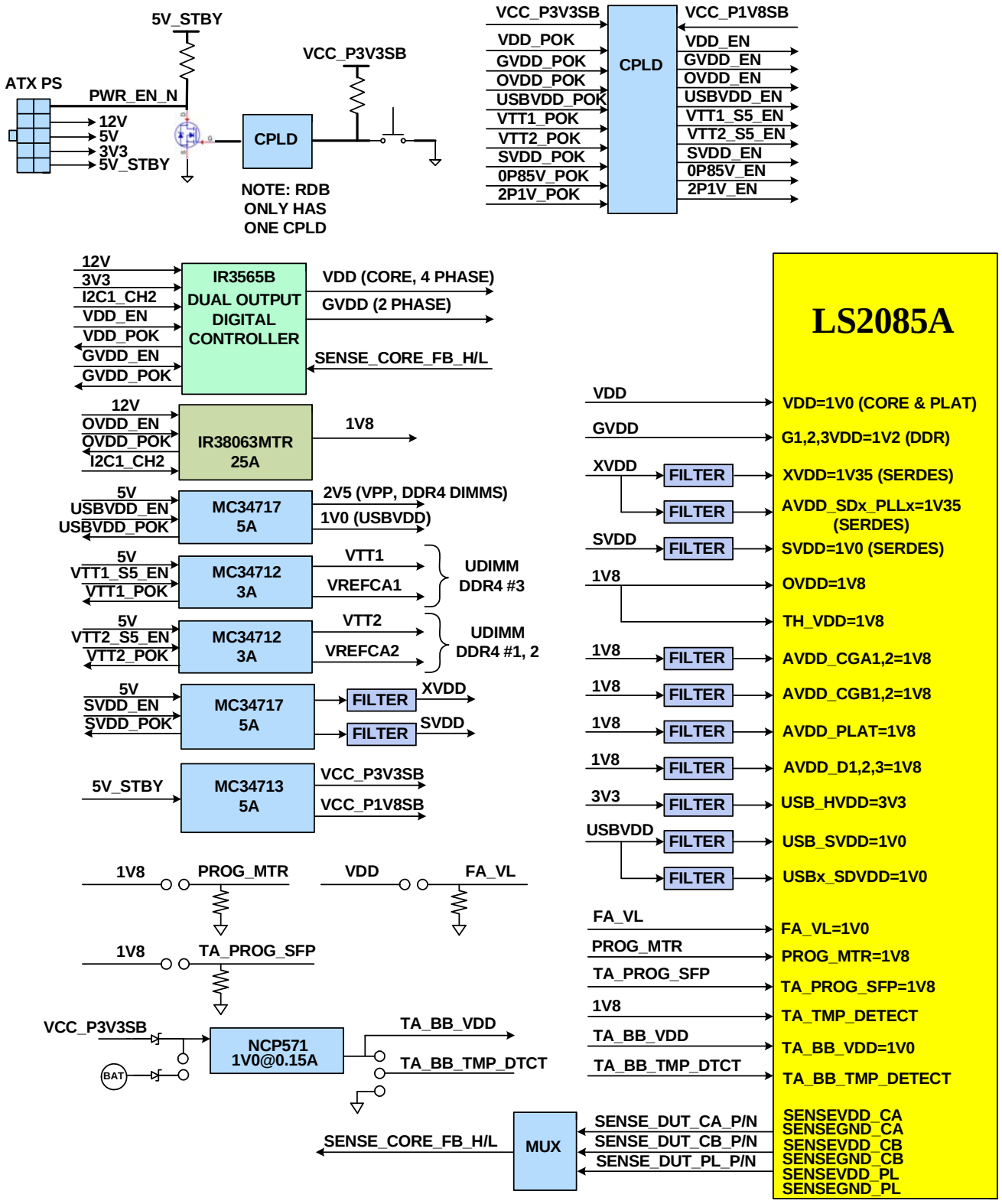
Table 2-15. Thermal monitor programming Setup

Configuration Action	Programming
Program Thermal limit to 105^0C	Set address 0x0B to 105 // Local Temp. High Limit = 105^0C Set address 0x0D to 105 // Ext. Temp. High Limit = 105^0C Set address 0x19,TLIMIT // Ext. THERM Limit = 105^0C Set address 0x20,TLIMIT // Local THERM Limit = 105^0C

2.9 Power supply (PS)

The LS2085A RDB PS provides all the voltages necessary for the correct operation of LS2085A device, x5 DDR4 uDIMMs, CPLD, AQUANTIA PHY, CORTINA PHY and all onboard peripher als. Figure 2-17 and Figure 2-18 details LS2085A RDB power supplies.

Figure 2-17. Power supply for LS2085A device



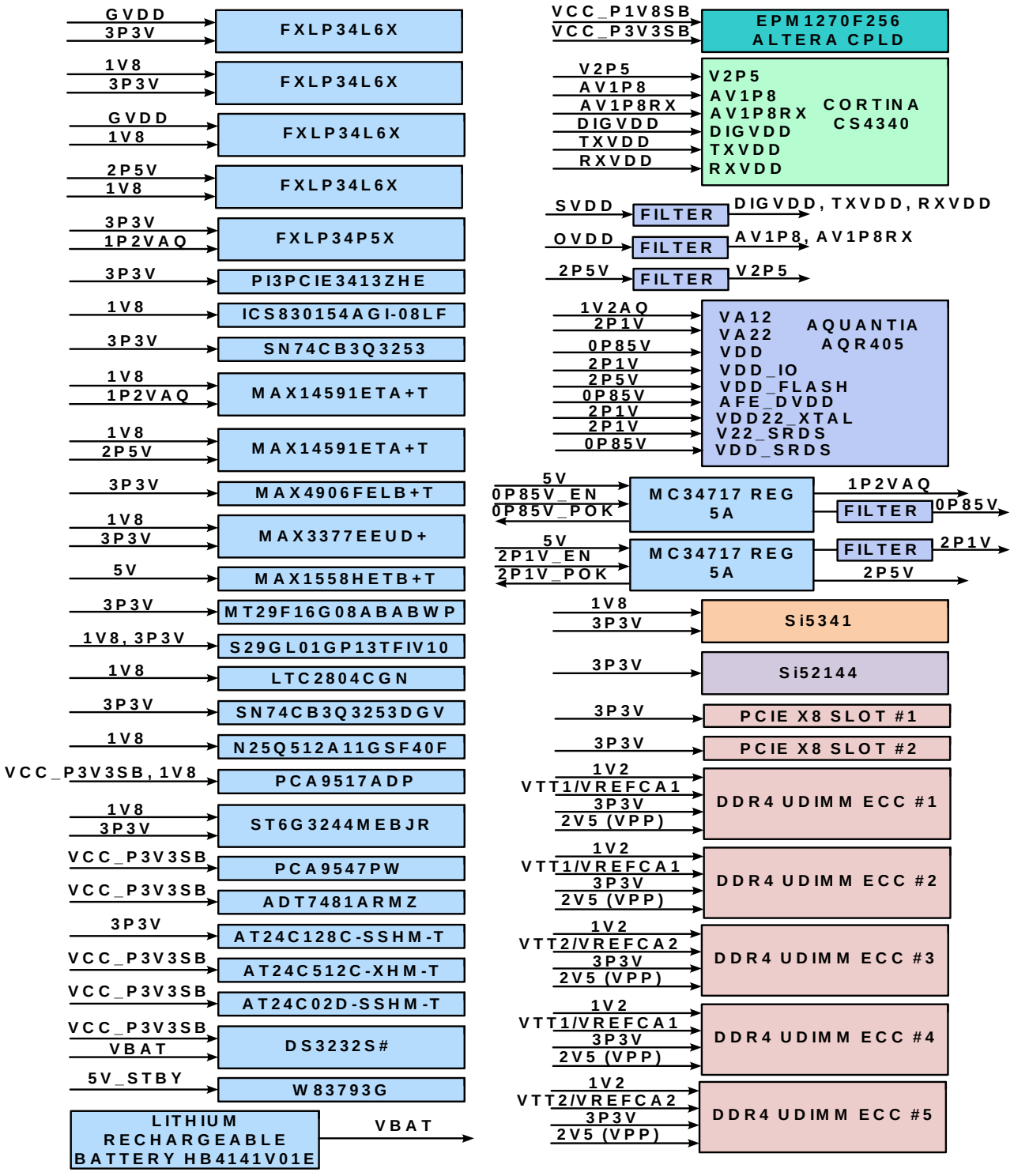


Figure 2-18. LS2085A RDB power for other devices

2.9.1 Primary power supply

The external ATX12V/EPS12V PS is a standard primary power supply (PC ATX-PS < 300W).

Table 2-16. Primary power supply

Power Supply	Description	
External ATX12V PS	Vin	90 - 264Vac
	Fin Frequency	50 - 60 Hz
	Iin	≤ 8.5A @100Vac, 4A @240Vac
	Power Good	Power-on delay time of 100 ~ 500ms
	Temperature Range	Operating: 0° ~ 50°C on full load
	Relative Humidity	20~ 80%

Table 2-17. ATX12V/EPS12 power supply output voltages

Group	1				2
VOLTAGE	+3.3V	+5V	+12V	-12V	+5VSB
MAX.LOAD	17A	18A	24A	0.3.A	2.5A
MIN.LOAD	0.5A	1A	2A	0A	0.1A
REGULATION	±5%	±5%	±5%	±10%	±5%
RIPPLE and NOISE (mV)	60	60	120	120	50
Capacitive Loads_(uF)	10000	10000	10000	330	10000

2.9.2 LS2085A RDB power supply structure

Table 2-18 lists power supply devices. Devices include visual indications and power sequence functions.

Table 2-18. LS2085A RDB power supply devices

Vendor	Device	Description
International Rectifier	IR3565B	DC-DC converter that produces: • LS2085A VDD voltage for cores and platform • LS2085A GVDD for all DDR controllers and x5 DDR uDIMMs The features are: • Vin = 12V • Vout = 1.0V +/-0.5% @ 60A, 1.2V +/-0.5% @ 30A • VID based PM Control
Freescale	MC34712	Regulator that produces DDR-related voltages: • DDR4 VREFCA 0.6V @ 10mA • DDR4 VTT 0.6V @ 3A There are two parts - one for DDR ports #1-2 and second for DDR port #3.

Table 2-18. LS2085A RDB power supply devices

Vendor	Device	Description
Freescale	MC34717	Regulator that produces DDR-related voltage: • DDR4 VPP 2.5V @ 1.5A There is one part for DDR ports #1,2 and 3.
Freescale	MC34717	POL regulator provides the following: • LS2085A XVDD for SerDes transceivers • LS2085A AVDD SerDes PLL's • 1.35-1.5V @ 3A
Freescale	MC34717	POL regulator produces LS2085A SVDD for SerDes Core voltage: 0.8-1.2V @ 2A
Freescale	MC34717	POL regulator provides the following: • LS2085A SXVDD for USB transceivers • LS2085A SPVDD USB PLL's • LS2085A SDVDD for USB core • 0.8 - 1.2V @ 2A
International Rectifier	IR38060MTRPbF	DC-DC Regulator provides the following: • LS2085A OVDD voltage for DMA, MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage • 1.8V @ 25A • VID based PM bus control • NOTE: If LS2085 (OVDD) and other devices that require1.8V consume less than 5A, then the MC34717 device should be used
On-Semiconductor	NCP571	Linear regulator produces LS2085A VDD_LP for Low Power Security Monitor supply: 1V @ 0.15A
FAIRCHILD	FDC6330L	Integrated load switches (3) provide ATX PS preload if CPU is absent or in low power mode.
Maxim	MAX1558HETB+	• USB VBUS Charge-pump
Freescale	MC34717	• POL regulator produces AQ2104 VA12 power rail: • 1.2V @ 360mA
Freescale	MC34717	• POL regulator produces AQ2104 VA22 & VDD_IO power rail: • 2.1V @ 450mA+TBD
Freescale	MC34717	• POL regulator produces AQ2104 VDD power rail: • 0.87V @ 3A
Freescale	MC34717	• POL regulator produces AQ2104 VDD_FLASH power rail: • 2.5V @ 20mA
Altera	EPM1270F256C5N CPLD	Control circuits, based on the Altera system control device, provide the following: • Reset • VDD/GVDD enable functionality • Visual indication.

2.9.3 LS2085A RDB power supply operation

2.9.3.1 Power-ON

The switch, SW1, which is on the front panel will cause the CPLD to enable the ATX supply for the onboard 3.3V, 5V and 12V powers.

2.9.3.2 Sequencing

After 3.3V, 5V and 12V become available on the board, all the power rails feeding the LS2085A will be automatically turned on and sequenced by the CPLD. Core VDD will be enabled first and then GVDD after that.

2.9.4 Voltage regulation

2.9.4.1 Platform, PLL, and Core

Set the default value of VDD and GVDD voltages by programming the IR3565B using a Remote I2C1_CH2 IR Programmer connector (JP17).

2.9.4.2 DDR

In Power-ON state, the DDR SDRAM termination (M_VTT), and reference (M_VREF) voltages are automatically set at the noted limits:

- DDR4 default GVDD = 1.2V
- M_VTT = 0.6V
- M_VREF = 0.6V

2.9.4.3 SVDD / XVDD

SVDD voltage has the following characteristics:

- Powers the core SERDES block
- Voltage value is set to 1.00V

XVDD voltage has the following characteristics:

- Powers the SERDES block IO
- Voltage value is set to 1.35V

Both SVDD and XVDD power is derived from a single dual ouput regulator UP13.

2.9.4.4 POVDD

POVDD voltage has the following characteristics:

- Possible to set to 0 V or 1.8 V

- J13 and J12 connects POVDD power line to LS2085A PROG_MTR and PROG_SFP pins. Otherwise, they will be pulled down to the Ground plane.

2.9.4.5 OVDD

OVDD (general IO) voltage is set to 1.8 V.

2.9.4.6 USB

USB voltages have the following characteristics:

- LS2085A USB PHY transceiver: USB_HVDD voltage is set to 3.3 V
- LS2085A USB PHY PLL: USB_SPVDD voltage is set to 1.0 V
- LS2085A USB PHY Analog: USB_SDVDD voltage is set to 1.0 V
- LS2085A USB PHY Transmit: USB_SXVDD voltage is set to 1.0 V
- External periphery device power: USB1_VBUS, USB2_VBUS voltage = 5 V corresponds to enable of USB1_DRVVBUS, USB2_DRVVBUS signal; otherwise, [default] USB_VBUS = 0 V

2.9.5 Power supply software control

Some of the power supplies can be adjusted by software as described in Table 2-19.

Table 2-19. Power supply software control

Power Supply	Adjustment method
VDD	PMBus
GVDD	PMBus
OVDD	PMBus

Through the LS2085A device and I2C1 port, core VDD and GVDD voltages can be adjusted through software.

2.10 USB interface

The LS2085A implements dual HS USB PHY's. Following are the main features:

- Compliance with USB Specification, USB Rev. 3.0
- Supports SS, HS, FS, and LS modes of operation
- Supports signalling
- Supports Host and OTG modes
  - — Working in Host or OTG mode (CN1 dependent), the RDB connects the 1st USB transceiver to connector Type A, thus enabling communication with keyboards, mice, memory sticks, and so on.

— Working in OTG mode, a 2nd USB port (CN2) connects to connector MicroAB and the MicroAB ID bus signal connects directly to the LS2085A internal PHY.

USB1_DRVVBUS and USB2_DRVVBUS control the VBUS Drive for both USB ports. USB1_PWRFAULT and USB2_PWRFAULT get Power Fault indications through Programmable-Current USB switch MAX1558H from Maxim. Maximum allowed current consumption of an USB connected device is 1.2A per channel.

Figure 2-19 shows the LS2085A RDB USB interface.

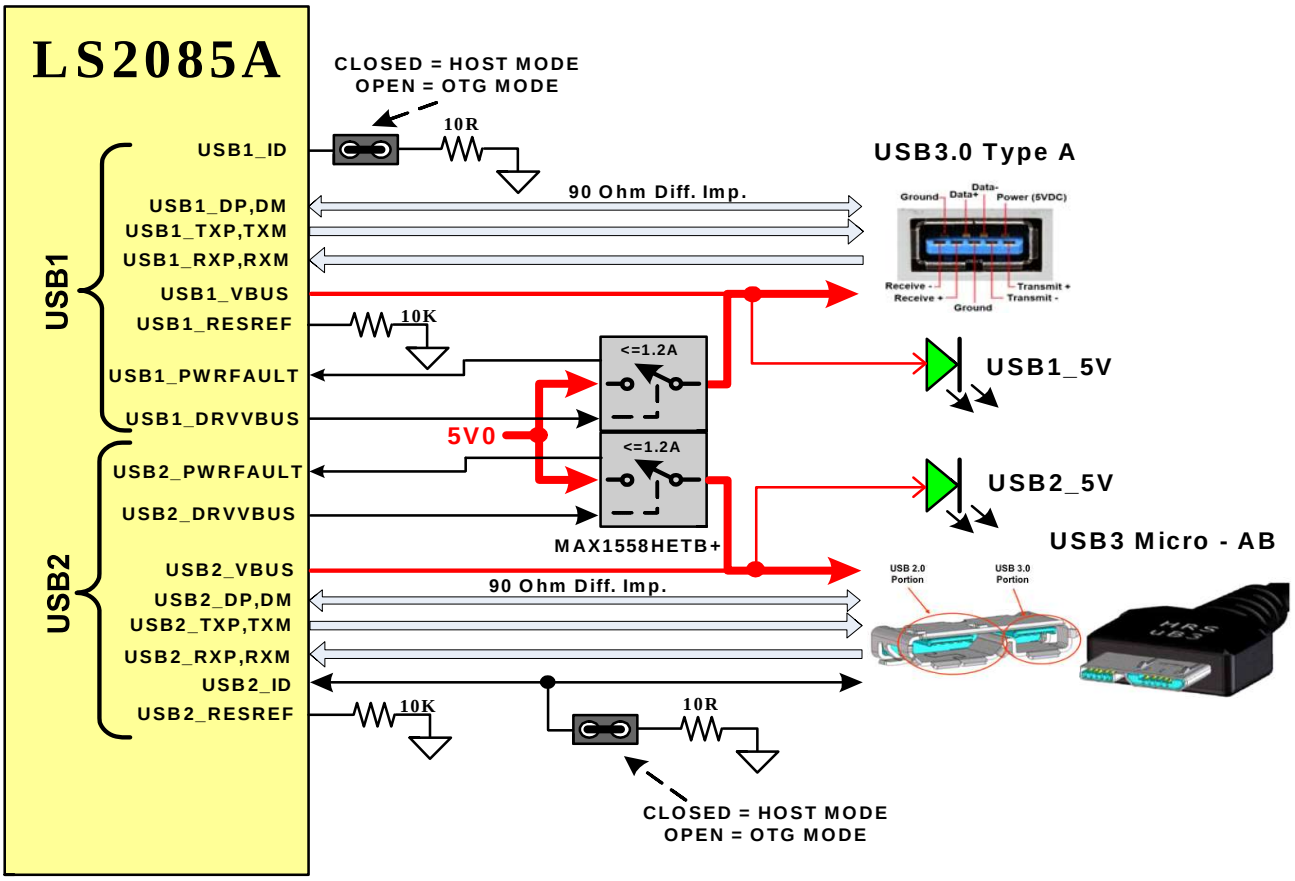


Figure 2-19. USB architecture

2.11 MPIC interrupt controller

LS2085A MPIC pins are connected to several devices on board. Connection to the Interrupt sources are done through voltage level shifters. LS2085A MPIC assignments are listed in Table 2-20.

In addition, the thermal monitor (U24) THERM_WARN_B and THERM_FAULT_B signals are driven into the CPLD. These are active low alert that can be programmed to assert if temperature or over current is achieved. In this case, the CPLD turns OFF all DUT power supplies.

Table 2-20. LS2085A interrupt assignments

Signal Name	Supported Functions	Description
IRQ0_B	CPLD Interrupt 1	
IRQ1_B	10G ETHERNET PHY Interrupt	AQR405 PHY0 Interrupt
IRQ2_B	10G ETHERNET PHY Interrupt	AQR405 PHY 1 Interrupt
IRQ3_B	CPLD Interrupt 2	Thermal Warning Interrupt
IRQ4_B	10G ETHERNET PHY Interrupt	AQR405 PHY 2 Interrupt
IRQ5_B	10G ETHERNET PHY Interrupt	AQR405 PHY 3 Interrupt
IRQ6_B	RTC	Real Time Clock Interrupt
IRQ7_B	PHY #4 Interrupt	CS4340 XFI Interrupt
IRQ8_B	10G_LAN_LED1	10G ETHERNET TRAFFIC LED INDICATOR 1
IRQ9_B	10G_LAN_LED2	10G ETHERNET TRAFFIC LED INDICATOR 1
IRQ10_B	10G_LAN_LED3	10G ETHERNET TRAFFIC LED INDICATOR 1
IRQ11_B	10G_LAN_LED4	10G ETHERNET TRAFFIC LED INDICATOR 1

2.12 Control group

LS2085A RDB controls group signals are required to configure the board for the required functionality.

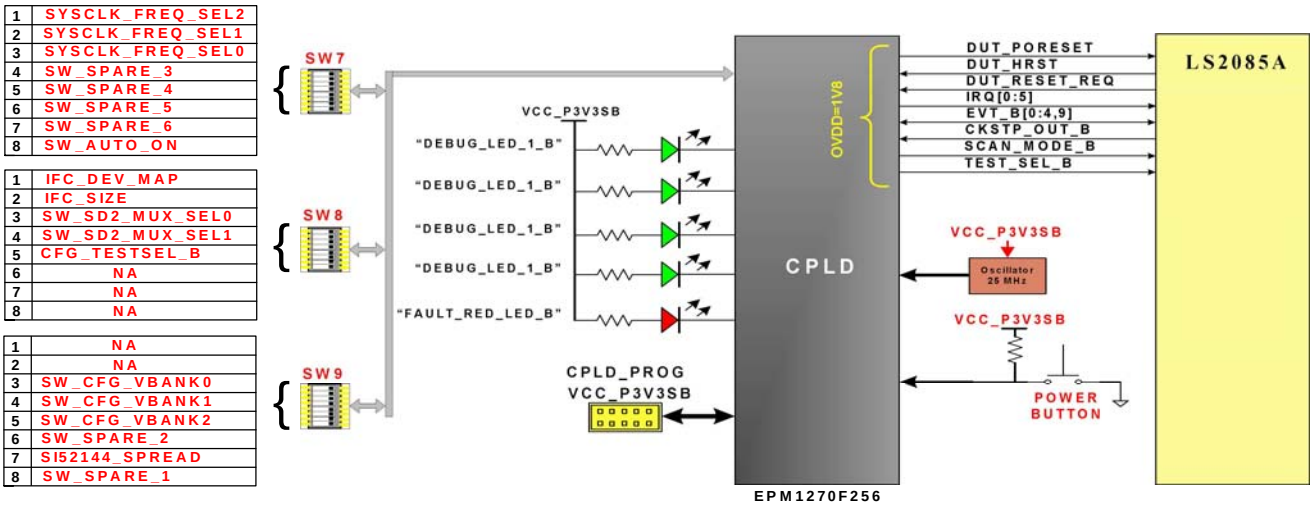


Figure 2-20. LS2085A RDB control

2.12.1 System control logic

LS2085A RDB contains a CPLD that implements the following functions:

- Resets sequencing/timing for ARM/JTAG, PCIe slots, DDR DIMMs, 1588 header, CS4340 PHY, AQR405 PHY, x4 and x8 PEX connector
- Power sequencing for LS2085 regulators including core VDD and GVDD
- Maps/re-maps LS2085A local bus chip selects to NOR and NAND Flash
- Translates switch settings into map/re-map for local bus chip select
- 1.8V to 3.3V translation for IFC signals going to the NAND Flash
- Providing NOR flash address bits A[11:25] from IFC address bus
- Serdes mux configuration
- Boot configuration
- Thermal fault control
- Fault management with inputs from Hardware Monitor device W83793G
- SYSCLK configuration
- Getting inputs from DIP switches
- Turns on the ATX power supply when power switch is pressed
- LED status control

The CPLD is powered from the local power supplies and clock input from an independent oscillator. This allows the CPLD to control all aspects of board bring-up, including memory and reset.

The CPLD is implemented in an Altera EPM1270F256 256-ball micro-BGA.

2.12.2 LS2085A Power-On Reset

LS2085A control group signals are basically used to stop or restart an execution. Figure 2-21 gives the connections overview and shows the Power-On Reset (POR) flow, while Table 2-21 outlines the POR sequence.

LS2085A HRST is a bi-directional open drain signal.

NOTE

Reset configuration input signals are ONLY sampled at the negation of POR. Reset Configuration input pins like CFG_RCW_SRC[0..8], CFG_SVR[0..1], CFG_GPINPUT[0..7], CFG_ENG_USE[0..2], CFG_DRAM_TYPE, functions differently when a device is not in a reset state.

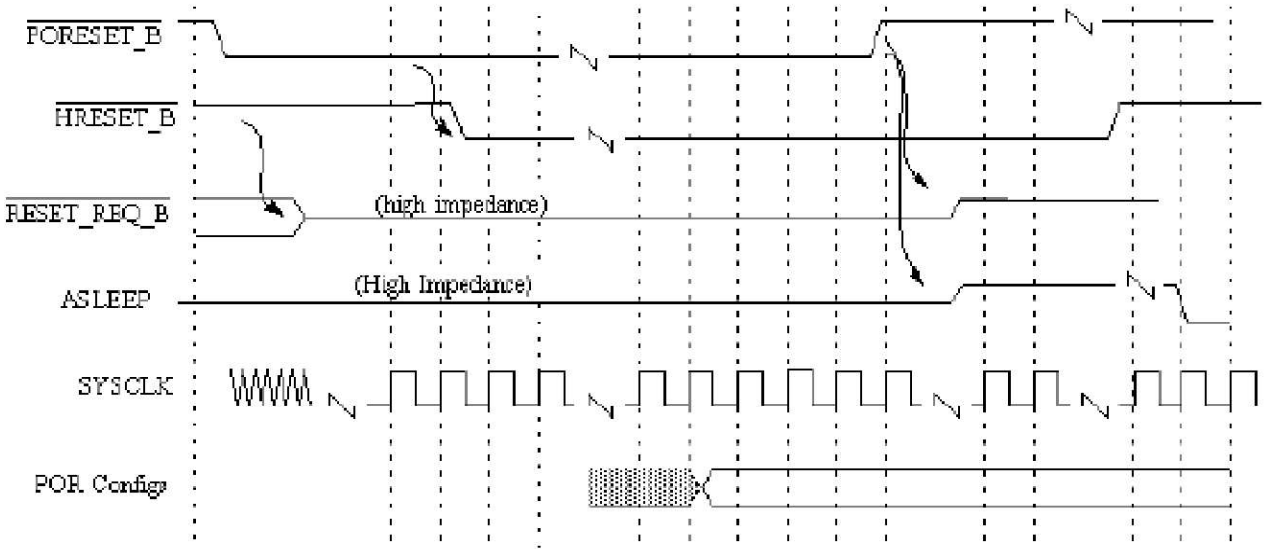


Figure 2-21. POR flow

Table 2-21. PORESET sequence

Step	Sequence Stage	Description
1	PORESET: General Information	• PORESET is asserted • CPLD drives CFG_RCW_SRC[0..8] and all reset configuration input signals to LS2085A; see Table 2-22 • CPLD de-assert PORESET and LS2085A samples the config pins. • LS2085A asserts HRESET and loads RCWs • LS2085A loads the RCW during HRESET • Once RCW load is complete, LS2085A de-asserts HRESET.
2	PORESET: During Negation	• LS2085A samples the configuration signals determines the interface to load the RCW • LS2085A asserts HRESET throughout PORESET
3	PORESET: After Negation	• LS2085A begins the configuration process and starts loading the RCW

Table 2-21. $\overline{\text{PORESET}}$ sequence

Step	Sequence Stage	Description
4	POR Configuration Input	Reset configuration inputs are sampled to determine the following: • Configuration source: CFG_RCW_SRC[0..8] • CFG_ENG_USE[0..2] • CFG_PLL_CONFIG_SEL_B • CFG_POR_AINIT • CFG_SOC_USE • CFG_GPINPUT[0:3] • DRAM Type Select (DDR3 or DDR3L): CFG_DRAM_TYPE • General Purpose Input: CFG_GPINPUT[0..7]. Only two[0..1] are driven • Response Disable: CFG_RSP_DIS • System Version Register: CFG_SVR[0..1] • CFG_IFC_TE
5	RCW Configuration Time	Time required varies according to RCW source and CLKIN frequency

NOTE

The LS2085A RDB has default DIP-switch settings that can be manually repositioned as per user selected configuration levels.

Table 2-22 describes the reset configuration input signals.

Table 2-22. LS2085A Reset configuration input signals

LS2085A Configuration Signal	LS2085A Pin Location	DIP SWITCH Preset	Description
CFG_RCW_SRC0	IFC_CLE	DIP-SW4[1]	Specifies RCW fetch location
CFG_RCW_SRC1	IFC_AD8	DIP-SW3[8]	Specifies RCW fetch location
CFG_RCW_SRC2	IFC_AD9	DIP-SW3[7]	Specifies RCW fetch location
CFG_RCW_SRC3	IFC_AD10	DIP-SW3[6]	Specifies RCW fetch location
CFG_RCW_SRC4	IFC_AD11	DIP-SW3[5]	Specifies RCW fetch location
CFG_RCW_SRC5	IFC_AD12	DIP-SW3[4]	Specifies RCW fetch location
CFG_RCW_SRC6	IFC_AD13	DIP-SW3[3]	Specifies RCW fetch location
CFG_RCW_SRC7	IFC_AD14	DIP-SW3[2]	Specifies RCW fetch location
CFG_RCW_SRC8	IFC_AD15	DIP-SW3[1]	Specifies RCW fetch location
CFG_ENG_USE0	IFC_WE_0_B	DIP-SW5[4]	
CFG_ENG_USE1	IFC_OE_B	DIP-SW5[3]	
CFG_ENG_USE2	IFC_WP_0_B	DIP-SW5[2]	
CFG_PLL_CONFIG_SEL_B	IFC_A2	DIP-SW4[3]	
CFG_POR_AINIT	IFC_A3	DIP-SW4[4]	
CFG_SOC_USE	ASLEEP	DIP-SW5[1]	
CFG_DRAM_TYPE	IFC_A5	DIP-SW4[7]	Specifies DRAM TYPE
CFG_GPINPUT0	IFC_AD0	DIP-SW5[8]	User defined

Table 2-22. LS2085A Reset configuration input signals

LS2085A Configuration Signal	LS2085A Pin Location	DIP SWITCH Preset	Description
CFG_GPINPUT1	IFC_AD1	DIP-SW5[7]	User defined
CFG_GPINPUT2	IFC_AD2	DIP-SW5[6]	
CFG_GPINPUT3	IFC_AD3	DIP-SW5[5]	
CFG_RSP_DIS	IFC_ALE	DIP-SW4[8]	Pause after fetching RCW
CFG_SVR0	IFC_A0	DIP-SW4[5]	
CFG_SVR1	IFC_A1	DIP-SW4[6]	
CFG_IFC_TE	IFC_TE	DIP-SW4[2]	IFC_TE signal enabled. Not used in Normal operation.

2.12.3 LS2085A RDB Reset

The reset signals sent to and from the LS2085A and other devices on LS2085A RDB are managed by a CPLD. Figure 2-22 shows an overview of the reset architecture.

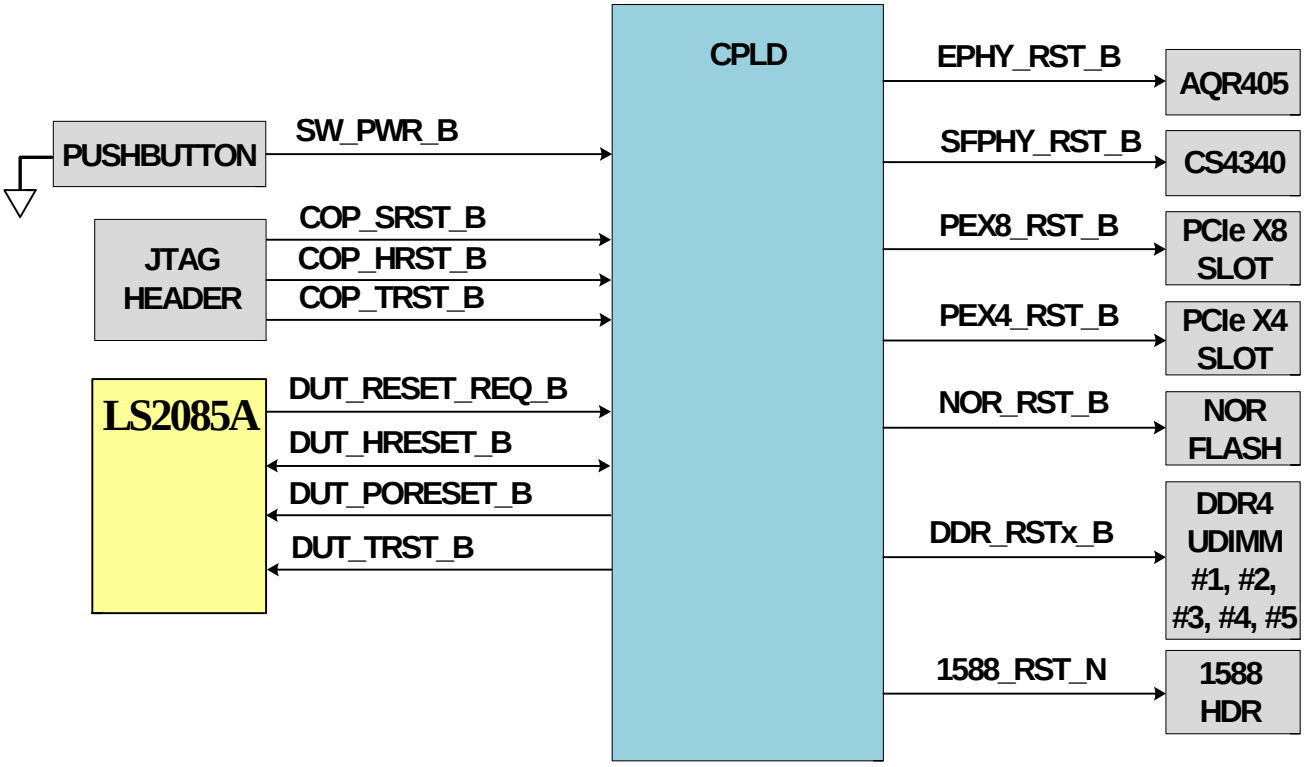


Figure 2-22. Reset architecture

2.13 JTAG port

The ARM/JTAG architecture is shown in Figure 2-23.

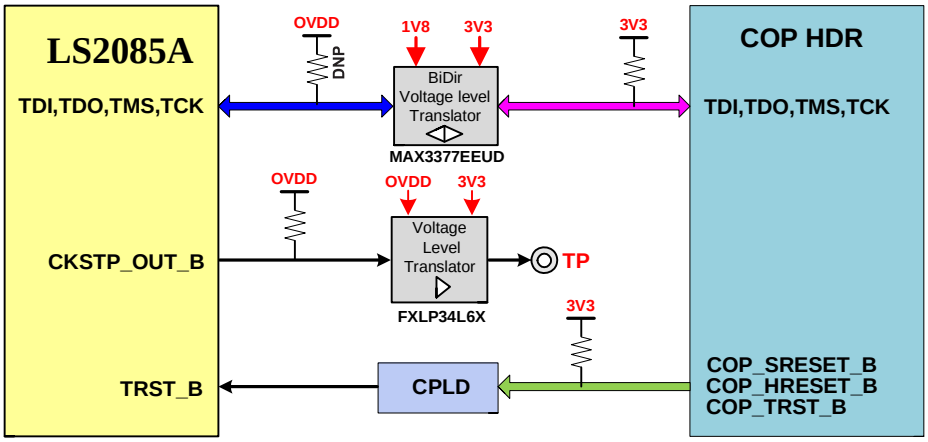


Figure 2-23. JTAG/COP connections

The CodeWarrior TAP will be used to communicate externally with the LS2085A through the RDB JTAG header JP10.

Legacy ARM HRST is mapped to the LS2085A POR. Legacy ARM SRST is mapped to the LS2085A HRESET.

2.14 GPIO pins

LS2085A has no dedicated GPIO pins. Instead, GPIO functions are multiplexed internally on other signals, which must be disabled before using the GPIO functions. GPIO is not needed for board operation. Most of the GPIO pin is not available for external access since the pin primary function is utilised. Some GPIO pins are connected to a testpoint to allow access. GPIO_4[6] to GPIO_4[9] can be used to drive four LED signals. The names of the GPIO pin with and without testpoint access are shown in Table 2-23.

Table 2-23. GPIO mapping

LS2085A Primary Function	LS2085A GPIO Function	Connection	Notes
IRQ[3]	GPIO_3[27]	CPLD	Has testpoint
IRQ[4]	GPIO_3[28]	AQR405 P2_INT_N	No testpoint
IRQ[5]	GPIO_3[29]	AQR405 P3_INT_N	No testpoint
IRQ[6]	GPIO_4[4]	RTC IRQ	No testpoint
IRQ[7]	GPIO_4[5]	CS4340 INT	No testpoint
IRQ[8]	GPIO_4[6]	10G LAN LED GPIO0	No testpoint
IRQ[9]	GPIO_4[7]	10G LAN LED GPIO1	No testpoint
IRQ[10]	GPIO_4[8]	10G LAN LED GPIO2	No testpoint

Table 2-23. GPIO mapping

LS2085A Primary Function	LS2085A GPIO Function	Connection	Notes
IRQ[11]	GPIO_4[9]	10G LAN LED GPIO3	No testpoint
EVT_B[9]	GPIO_4[10]	UNUSED	Has testpoint
ASLEEP	GPIO_1[28]	CPLD	Has testpoint
RTC	GPIO_3[30]	RTC CLK	Has testpoint